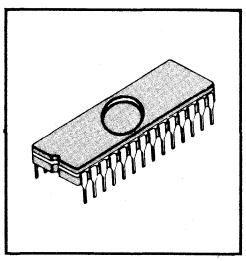
SAMSUNG

Data Book

CPL™

(CMOS Programmable Logic)

1989



CMOS PROGRAMMABLE LOGIC (CPL™)

Data Book

SECOND EDITION

1989 SAMSUNG
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INTRODUCTION

Samsung's CMOS Programmable Logic (CPL™) family introduces the benefits of advanced CMOS technology into the field programmable logic area, allowing system designers to save significant amounts of power without compromising performance.

The first generation of CPL devices, as specified in this book, are CMOS implementations of the industry standard PAL® devices. The 1.2 micron CMOS EPROM technology allows CPL parts to achieve bipolar performance at a much lower power, resulting in reduced system costs and easier prototyping. The erasable EPROM cell also facilitates 100% functional and AC testing of every part before it is released to market, making possible 100% programming yields.

Programming CPL devices is done by using standard PLD programmers. Because of the architectural compatibility with bipolar PAL devices, all current software tools also support the CPL devices. Therefore, no modification in the code is necessary when replacing a bipolar PAL device with a CPL device.

PAL® is a registered trademark of Monolithic Memories Inc.

Product Guide 1

Technical Overview/Quality and Reliability 2

Product Specifications 3

CPL Programming Electrical Specifications 4

CPL Starter Kit/CPL Programmer and Software Guide 5

Definition of Terms 6

Package Drawings 7

Sales Offices 8

SAMSUNG
Electronics

Product Guide 1

Technical Overview/Quality and Reliability 2

Product Specifications 3

CPL Programming Electrical Specifications 4

CPL Starter Kit/CPL Programmer and Software Guide 5

Definition of Terms 6

Package Drawings 7

Sales Offices 8

SAMSUNG
Electronics

PRODUCT INDEX

PRODUCT DESIGNATION	DESCRIPTION	PAGES
CPL16L8L-15NC	OTP, Plastic 20-pin, 1/4 Power, 15ns, CMOS PLD, Comm.	29-37
CPL16L8L-15NLC	20-pin PLCC, 1/4 Power, 15ns, CMOS PLD, Comm.	29-37
CPL16L8L-15WC	20-pin Windowed CERDIP, 1/4 Power, 15ns, CMOS PLD, Comm.	29-37
CPL16L8-15NC	OTP, Plastic 20-pin, 1/2 Power, 15ns, CMOS PLD, Comm.	29-37
CPL16L8-15NLC	20-pin PLCC, 1/2 Power, 15ns, CMOS PLD, Comm.	29-37
CPL16L8L-20NC	OTP, Plastic 20-pin, 1/4 Power, 20ns, CMOS PLD, Comm.	29-37
CPL16L8L-20NLC	20-pin PLCC, 1/4 Power, 20ns, CMOS PLD, Comm.	29-37
CPL16L8L-20WC	20-pin Windowed CERDIP, 1/4 Power, 20ns, CMOS PLD, Comm.	29-37
CPL16L8-20NC	OTP, Plastic 20-pin, 1/2 Power, 20ns, CMOS PLD, Comm.	29-37
CPL16L8-20NLC	20-pin PLCC, 1/2 Power, 20ns, CMOS PLD, Comm.	29-37
CPL16L8L-25NC	OTP, Plastic 20-pin, 1/4 Power, 25ns, CMOS PLD, Comm.	29-37
CPL16L8L-25NLC	20-pin PLCC, 1/4 Power, 25ns, CMOS PLD, Comm.	29-37
CPL16L8L-25WC	20-pin Windowed CERDIP, 1/4 Power, 25ns, CMOS PLD, Comm.	29-37
CPL16L8L-25NI	OTP, Plastic 20-pin, 1/4 Power, 25ns, CMOS PLD, Ind.	29-37
CPL16L8-25NC	OTP, Plastic 20-pin, 1/2 Power, 25ns, CMOS PLD, Comm.	29-37
CPL16L8-25NLC	20-pin PLCC, 1/2 Power, 25ns, CMOS PLD, Comm.	29-37
CPL16L8L-35NC	OTP, Plastic 20-pin, 1/4 Power, 35ns, CMOS PLD, Comm.	29-37
CPL16L8L-35NLC	20-pin PLCC, 1/4 Power, 35ns, CMOS PLD, Comm.	29-37
CPL16L8-35NC	OTP, Plastic 20-pin, 1/2 Power, 35ns, CMOS PLD, Comm.	29-37
CPL16L8-35NLC	20-pin PLCC, 1/2 Power, 35ns, CMOS PLD, Comm.	29-37
CPL16R4L-15NC	OTP, Plastic 20-pin, 1/4 Power, 15ns, CMOS PLD, Comm.	29-37
CPL16R4L-15NLC	20-pin PLCC, 1/4 Power, 15ns, CMOS PLD, Comm.	29-37
CPL16R4L-15WC	20-pin Windowed CERDIP, 1/4 Power, 15ns, CMOS PLD, Comm.	29-37
CPL16R4-15NC	OTP, Plastic 20-pin, 1/2 Power, 15ns, CMOS PLD, Comm.	29-37
CPL16R4-15NLC	20-pin PLCC, 1/2 Power, 15ns, CMOS PLD, Comm.	29-37
CPL16R4L-20NC	OTP, Plastic 20-pin, 1/4 Power, 20ns, CMOS PLD, Comm.	29-37
CPL16R4L-20NLC	20-pin PLCC, 1/4 Power, 20ns, CMOS PLD, Comm.	29-37
CPL16R4L-20WC	20-pin Windowed CERDIP, 1/4 Power, 20ns, CMOS PLD, Comm.	29-37
CPL16R4-20NC	OTP, Plastic 20-pin, 1/2 Power, 20ns, CMOS PLD, Comm.	29-37
CPL16R4-20NLC	20-pin PLCC, 1/2 Power, 20ns, CMOS PLD, Comm.	29-37

PRODUCT INDEX

PRODUCT DESIGNATION	DESCRIPTION	PAGES
CPL16R4L-25NC	OTP, Plastic 20-pin, 1/4 Power, 25ns, CMOS PLD, Comm.	29-37
CPL16R4L-25NLC	20-pin PLCC, 1/4 Power, 25ns, CMOS PLD, Comm.	29-37
CPL16R4L-25WC	20-pin Windowed CERDIP, 1/4 Power, 25ns, CMOS PLD, Comm.	29-37
CPL16R4L-25NI	OTP, Plastic 20-pin, 1/4 Power, 25ns, CMOS PLD, Ind.	29-37
CPL16R4-25NC	OTP, Plastic 20-pin, 1/2 Power, 25ns, CMOS PLD, Comm.	29-37
CPL16R4-25NLC	20-pin PLCC, 1/2 Power, 25ns, CMOS PLD, Comm.	29-37
CPL16R4L-35NC	OTP, Plastic 20-pin, 1/4 Power, 35ns, CMOS PLD, Comm.	29-37
CPL16R4L-35NLC	20-pin PLCC, 1/4 Power, 35ns, CMOS PLD, Comm.	29-37
CPL16R4-35NC	OTP, Plastic 20-pin, 1/2 Power, 35ns, CMOS PLD, Comm.	29-37
CPL16R4-35NLC	20-pin PLCC, 1/2 Power, 35ns, CMOS PLD, Comm.	29-37
CPL16R6L-15NC	OTP, Plastic 20-pin, 1/4 Power, 15ns, CMOS PLD, Comm.	29-37
CPL16R6L-15NLC	20-pin PLCC, 1/4 Power, 15ns, CMOS PLD, Comm.	29-37
CPL16R6L-15WC	20-pin Windowed CERDIP, 1/4 Power, 15ns, CMOS PLD, Comm.	29-37
CPL16R6-15NC	OTP, Plastic 20-pin, 1/2 Power, 15ns, CMOS PLD, Comm.	29-37
CPL16R6-15NLC	20-pin PLCC, 1/2 Power, 15ns, CMOS PLD, Comm.	29-37
CPL16R6L-20NC	OTP, Plastic 20-pin, 1/4 Power, 20ns, CMOS PLD, Comm.	29-37
CPL16R6L-20NLC	20-pin PLCC, 1/4 Power, 20ns, CMOS PLD, Comm.	29-37
CPL16R6L-20WC	20-pin Windowed CERDIP, 1/4 Power, 20ns, CMOS PLD, Comm.	29-37
CPL16R6-20NC	OTP, Plastic 20-pin, 1/2 Power, 20ns, CMOS PLD, Comm.	29-37
CPL16R6-20NLC	20-pin PLCC, 1/2 Power, 20ns, CMOS PLD, Comm.	29-37
CPL16R6L-25NC	OTP, Plastic 20-pin, 1/4 Power, 25ns, CMOS PLD, Comm.	29-37
CPL16R6L-25NLC	20-pin PLCC, 1/4 Power, 25ns, CMOS PLD, Comm.	29-37
CPL16R6L-25WC	20-pin Windowed CERDIP, 1/4 Power, 25ns, CMOS PLD, Comm.	29-37
CPL16R6L-25NI	OTP, Plastic 20-pin, 1/4 Power, 25ns, CMOS PLD, Ind.	29-37
CPL16R6-25NC	OTP, Plastic 20-pin, 1/2 Power, 25ns, CMOS PLD, Comm.	29-37
CPL16R6-25NLC	20-pin PLCC, 1/2 Power, 25ns, CMOS PLD, Comm.	29-37
CPL16R6L-35NC	OTP, Plastic 20-pin, 1/4 Power, 35ns, CMOS PLD, Comm.	29-37
CPL16R6L-35NLC	20-pin PLCC, 1/4 Power, 35ns, CMOS PLD, Comm.	29-37
CPL16R6-35NC	OTP, Plastic 20-pin, 1/2 Power, 35ns, CMOS PLD, Comm.	29-37
CPL16R6-35NLC	20-pin PLCC, 1/2 Power, 35ns, CMOS PLD, Comm.	29-37

PRODUCT INDEX

PRODUCT DESIGNATION	DESCRIPTION	PAGES
CPL16R8L-15NC	OTP, Plastic 20-pin, 1/4 Power, 15ns, CMOS PLD, Comm.	29-37
CPL16R8L-15NLC	20-pin PLCC, 1/4 Power, 15ns, CMOS PLD, Comm.	29-37
CPL16R8L-15WC	20-pin Windowed CERDIP, 1/4 Power, 15ns, CMOS PLD, Comm.	29-37
CPL16R8-15NC	OTP, Plastic 20-pin, 1/2 Power, 15ns, CMOS PLD, Comm.	29-37
CPL16R8-15NLC	20-pin PLCC, 1/2 Power, 15ns, CMOS PLD, Comm.	29-37
CPL16R8L-20NC	OTP, Plastic 20-pin, 1/4 Power, 20ns, CMOS PLD, Comm.	29-37
CPL16R8L-20NLC	20-pin PLCC, 1/4 Power, 20ns, CMOS PLD, Comm.	29-37
CPL16R8L-20WC	20-pin Windowed CERDIP, 1/4 Power, 20ns, CMOS PLD, Comm.	29-37
CPL16R8-20NC	OTP, Plastic 20-pin, 1/2 Power, 20ns, CMOS PLD, Comm.	29-37
CPL16R8-20NLC	20-pin PLCC, 1/2 Power, 20ns, CMOS PLD, Comm.	29-37
CPL16R8L-25NC	OTP, Plastic 20-pin, 1/4 Power, 25ns, CMOS PLD, Comm.	29-37
CPL16R8L-25NLC	20-pin PLCC, 1/4 Power, 25ns, CMOS PLD, Comm.	29-37
CPL16R8L-25WC	20-pin Windowed CERDIP, 1/4 Power, 25ns, CMOS PLD, Comm.	29-37
CPL16R8L-25NI	OTP, Plastic 20-pin, 1/4 Power, 25ns, CMOS PLD, Ind.	29-37
CPL16R8-25NC	OTP, Plastic 20-pin, 1/2 Power, 25ns, CMOS PLD, Comm.	29-37
CPL16R8-25NLC	20-pin PLCC, 1/2 Power, 25ns, CMOS PLD, Comm.	29-37
CPL16R8L-35NC	OTP, Plastic 20-pin, 1/4 Power, 35ns, CMOS PLD, Comm.	29-37
CPL16R8L-35NLC	20-pin PLCC, 1/4 Power, 35ns, CMOS PLD, Comm.	29-37
CPL16R8-35NC	OTP, Plastic 20-pin, 1/2 Power, 35ns, CMOS PLD, Comm.	29-37
CPL16R8-35NLC	20-pin PLCC, 1/2 Power, 35ns, CMOS PLD, Comm.	29-37
CPL20L8L-15NC	OTP, Plastic 24-pin, 1/4 Power, 15ns, CMOS PLD, Comm.	39-49
CPL20L8L-15NLC	24-pin PLCC, 1/4 Power, 15ns, CMOS PLD, Comm.	39-49
CPL20L8L-15WC	24-pin Windowed CERDIP, 1/4 Power, 15ns, CMOS PLD, Comm.	39-49
CPL20L8-15NC	OTP, Plastic 24-pin, 1/2 Power, 15ns, CMOS PLD, Comm.	39-49
CPL20L8-15NLC	24-pin PLCC, 1/2 Power, 15ns, CMOS PLD, Comm.	39-49
CPL20L8L-20NC	OTP, Plastic 24-pin, 1/4 Power, 20ns, CMOS PLD, Comm.	39-49
CPL20L8L-20NLC	24-pin PLCC, 1/4 Power, 20ns, CMOS PLD, Comm.	39-49
CPL20L8L-20WC	24-pin Windowed CERDIP, 1/4 Power, 20ns, CMOS PLD, Comm.	39-49
CPL20L8-20NC	OTP, Plastic 24-pin, 1/2 Power, 20ns, CMOS PLD, Comm.	39-49
CPL20L8-20NLC	24-pin PLCC, 1/2 Power, 20ns, CMOS PLD, Comm.	39-49

PRODUCT INDEX

PRODUCT DESIGNATION	DESCRIPTION	PAGES
CPL20L8L-25NC	OTP, Plastic 24-pin, 1/4 Power, 25ns, CMOS PLD, Comm.	39-49
CPL20L8L-25NLC	24-pin PLCC, 1/4 Power, 25ns, CMOS PLD, Comm.	39-49
CPL20L8L-25WC	24-pin Windowed CERDIP, 1/4 Power, 25ns, CMOS PLD, Comm.	39-49
CPL20L8L-25NI	OTP, Plastic 24-pin, 1/4 Power, 25ns, CMOS PLD, Ind.	39-49
CPL20L8-25NC	OTP, Plastic 24-pin, 1/2 Power, 25ns, CMOS PLD, Comm.	39-49
CPL20L8-25NLC	24-pin PLCC, 1/2 Power, 25ns, CMOS PLD, Comm.	39-49
CPL20L8L-35NC	OTP, Plastic 24-pin, 1/4 Power, 35ns, CMOS PLD, Comm.	39-49
CPL20L8L-35NLC	24-pin PLCC, 1/4 Power, 35ns, CMOS PLD, Comm.	39-49
CPL20L8-35NC	OTP, Plastic 24-pin, 1/2 Power, 35ns, CMOS PLD, Comm.	39-49
CPL20L8-35NLC	24-pin PLCC, 1/2 Power, 35ns, CMOS PLD, Comm.	39-49
CPL20R4L-15NC	OTP, Plastic 24-pin, 1/4 Power, 15ns, CMOS PLD, Comm.	39-49
CPL20R4L-15NLC	24-pin PLCC, 1/4 Power, 15ns, CMOS PLD, Comm.	39-49
CPL20R4L-15WC	24-pin Windowed CERDIP, 1/4 Power, 15ns, CMOS PLD, Comm.	39-49
CPL20R4-15NC	OTP, Plastic 24-pin, 1/2 Power, 15ns, CMOS PLD, Comm.	39-49
CPL20R4-15NLC	24-pin PLCC, 1/2 Power, 15ns, CMOS PLD, Comm.	39-49
CPL20R4L-20NC	OTP, Plastic 24-pin, 1/4 Power, 20ns, CMOS PLD, Comm.	39-49
CPL20R4L-20NLC	24-pin PLCC, 1/4 Power, 20ns, CMOS PLD, Comm.	39-49
CPL20R4L-20WC	24-pin Windowed CERDIP, 1/4 Power, 20ns, CMOS PLD, Comm.	39-49
CPL20R4-20NC	OTP, Plastic 24-pin, 1/2 Power, 20ns, CMOS PLD, Comm.	39-49
CPL20R4-20NLC	24-pin PLCC, 1/2 Power, 20ns, CMOS PLD, Comm.	39-49
CPL20R4L-25NC	OTP, Plastic 24-pin, 1/4 Power, 25ns, CMOS PLD, Comm.	39-49
CPL20R4L-25NLC	24-pin PLCC, 1/4 Power, 25ns, CMOS PLD, Comm.	39-49
CPL20R4L-25WC	24-pin Windowed CERDIP, 1/4 Power, 25ns, CMOS PLD, Comm.	39-49
CPL20R4L-25NI	OTP, Plastic 24-pin, 1/4 Power, 25ns, CMOS PLD, Ind.	39-49
CPL20R4-25NC	OTP, Plastic 24-pin, 1/2 Power, 25ns, CMOS PLD, Comm.	39-49
CPL20R4-25NLC	24-pin PLCC, 1/2 Power, 25ns, CMOS PLD, Comm.	39-49
CPL20R4L-35NC	OTP, Plastic 24-pin, 1/4 Power, 35ns, CMOS PLD, Comm.	39-49
CPL20R4L-35NLC	24-pin PLCC, 1/4 Power, 35ns, CMOS PLD, Comm.	39-49
CPL20R4-35NC	OTP, Plastic 24-pin, 1/2 Power, 35ns, CMOS PLD, Comm.	39-49
CPL20R4-35NLC	24-pin PLCC, 1/2 Power, 35ns, CMOS PLD, Comm.	39-49

PRODUCT INDEX

PRODUCT DESIGNATION	DESCRIPTION	PAGES
CPL20R6L-15NC	OTP, Plastic 24-pin, 1/4 Power, 15ns, CMOS PLD, Comm.	39-49
CPL20R6L-15NLC	24-pin PLCC, 1/4 Power, 15ns, CMOS PLD, Comm.	39-49
CPL20R6L-15WC	24-pin Windowed CERDIP, 1/4 Power, 15ns, CMOS PLD, Comm.	39-49
CPL20R6-15NC	OTP, Plastic 24-pin, 1/2 Power, 15ns, CMOS PLD, Comm.	39-49
CPL20R6-15NLC	24-pin PLCC, 1/2 Power, 15ns, CMOS PLD, Comm.	39-49
CPL20R6L-20NC	OTP, Plastic 24-pin, 1/4 Power, 20ns, CMOS PLD, Comm.	39-49
CPL20R6L-20NLC	24-pin PLCC, 1/4 Power, 20ns, CMOS PLD, Comm.	39-49
CPL20R6L-20WC	24-pin Windowed CERDIP, 1/4 Power, 20ns, CMOS PLD, Comm.	39-49
CPL20R6-20NC	OTP, Plastic 24-pin, 1/2 Power, 20ns, CMOS PLD, Comm.	39-49
CPL20R6-20NLC	24-pin PLCC, 1/2 Power, 20ns, CMOS PLD, Comm.	39-49
CPL20R6L-25NC	OTP, Plastic 24-pin, 1/4 Power, 25ns, CMOS PLD, Comm.	39-49
CPL20R6L-25NLC	24-pin PLCC, 1/4 Power, 25ns, CMOS PLD, Comm.	39-49
CPL20R6L-25WC	24-pin Windowed CERDIP, 1/4 Power, 25ns, CMOS PLD, Comm.	39-49
CPL20R6L-25NI	OTP, Plastic 24-pin, 1/4 Power, 25ns, CMOS PLD, Ind.	39-49
CPL20R6-25NC	OTP, Plastic 24-pin, 1/2 Power, 25ns, CMOS PLD, Comm.	39-49
CPL20R6-25NLC	24-pin PLCC, 1/2 Power, 25ns, CMOS PLD, Comm.	39-49
CPL20R6L-35NC	OTP, Plastic 24-pin, 1/4 Power, 35ns, CMOS PLD, Comm.	39-49
CPL20R6L-35NLC	24-pin PLCC, 1/4 Power, 35ns, CMOS PLD, Comm.	39-49
CPL20R6-35NC	OTP, Plastic 24-pin, 1/2 Power, 35ns, CMOS PLD, Comm.	39-49
CPL20R6-35NLC	24-pin PLCC, 1/2 Power, 35ns, CMOS PLD, Comm.	39-49
CPL20R8L-15NC	OTP, Plastic 24-pin, 1/4 Power, 15ns, CMOS PLD, Comm.	39-49
CPL20R8L-15NLC	24-pin PLCC, 1/4 Power, 15ns, CMOS PLD, Comm.	39-49
CPL20R8L-15WC	24-pin Windowed CERDIP, 1/4 Power, 15ns, CMOS PLD, Comm.	39-49
CPL20R8-15NC	OTP, Plastic 24-pin, 1/2 Power, 15ns, CMOS PLD, Comm.	39-49
CPL20R8-15NLC	24-pin PLCC, 1/2 Power, 15ns, CMOS PLD, Comm.	39-49
CPL20R8L-20NC	OTP, Plastic 24-pin, 1/4 Power, 20ns, CMOS PLD, Comm.	39-49
CPL20R8L-20NLC	24-pin PLCC, 1/4 Power, 20ns, CMOS PLD, Comm.	39-49
CPL20R8L-20WC	24-pin Windowed CERDIP, 1/4 Power, 20ns, CMOS PLD, Comm.	39-49
CPL20R8-20NC	OTP, Plastic 24-pin, 1/2 Power, 20ns, CMOS PLD, Comm.	39-49
CPL20R8-20NLC	24-pin PLCC, 1/2 Power, 20ns, CMOS PLD, Comm.	39-49

PRODUCT INDEX

PRODUCT DESIGNATION	DESCRIPTION	PAGES
CPL20R8L-25NC	OTP, Plastic 24-pin, 1/4 Power, 25ns, CMOS PLD, Comm.	39-49
CPL20R8L-25NLC	24-pin PLCC, 1/4 Power, 25ns, CMOS PLD, Comm.	39-49
CPL20R8L-25WC	24-pin Windowed CERDIP, 1/4 Power, 25ns, CMOS PLD, Comm.	39-49
CPL20R8L-25NI	OTP, Plastic 24-pin, 1/4 Power, 25ns, CMOS PLD, Ind.	39-49
CPL20R8-25NC	OTP, Plastic 24-pin, 1/2 Power, 25ns, CMOS PLD, Comm.	39-49
CPL20R8-25NLC	24-pin PLCC, 1/2 Power, 25ns, CMOS PLD, Comm.	39-49
CPL20R8-35NLC	OTP, Plastic 24-pin, 1/4 Power, 35ns, CMOS PLD, Comm.	39-49
CPL20R8L-35NC	24-pin PLCC, 1/4 Power, 35ns, CMOS PLD, Comm.	39-49
CPL20R8L-35NLC	OTP, Plastic 24-pin, 1/2 Power, 35ns, CMOS PLD, Comm.	39-49
CPL20R8-35NC	24-pin PLCC, 1/2 Power, 35ns, CMOS PLD, Comm.	39-49
CPL20L10L-15NC	OTP, Plastic 24-pin, 1/4 Power, 15ns, CMOS PLD, Comm.	39-49
CPL20L10L-15NLC	24-pin PLCC, 1/4 Power, 15ns, CMOS PLD, Comm.	39-49
CPL20L10L-15WC	24-pin Windowed CERDIP, 1/4 Power, 15ns, CMOS PLD, Comm.	39-49
CPL20L10-15NC	OTP, Plastic 24-pin, 1/2 Power, 15ns, CMOS PLD, Comm.	39-49
CPL20L10-15NLC	24-pin PLCC, 1/2 Power, 15ns, CMOS PLD, Comm.	39-49
CPL20L10L-20NC	OTP, Plastic 24-pin, 1/4 Power, 20ns, CMOS PLD, Comm.	39-49
CPL20L10L-20NLC	24-pin PLCC, 1/4 Power, 20ns, CMOS PLD, Comm.	39-49
CPL20L10L-20WC	24-pin Windowed CERDIP, 1/4 Power, 20ns, CMOS PLD, Comm.	39-49
CPL20L10-20NC	OTP, Plastic 24-pin, 1/2 Power, 20ns, CMOS PLD, Comm.	39-49
CPL20L10-20NLC	24-pin PLCC, 1/2 Power, 20ns, CMOS PLD, Comm.	39-49
CPL20L10L-25NC	OTP, Plastic 24-pin, 1/4 Power, 25ns, CMOS PLD, Comm.	39-49
CPL20L10L-25NLC	24-pin PLCC, 1/4 Power, 25ns, CMOS PLD, Comm.	39-49
CPL20L10L-25WC	24-pin Windowed CERDIP, 1/4 Power, 25ns, CMOS PLD, Comm.	39-49
CPL20L10L-25NI	OTP, Plastic 24-pin, 1/4 Power, 25ns, CMOS PLD, Ind.	39-49
CPL20L10-25NC	OTP, Plastic 24-pin, 1/2 Power, 25ns, CMOS PLD, Comm.	39-49
CPL20L10-25NLC	24-pin PLCC, 1/2 Power, 25ns, CMOS PLD, Comm.	39-49
CPL20L10L-30NC	OTP, Plastic 24-pin, 1/4 Power, 30ns, CMOS PLD, Comm.	39-49
CPL20L10L-30NLC	24-pin PLCC, 1/4 Power, 30ns, CMOS PLD, Comm.	39-49
CPL20L10-30NC	OTP, Plastic 24-pin, 1/2 Power, 30ns, CMOS PLD, Comm.	39-49
CPL20L10-30NLC	24-pin PLCC, 1/2 Power, 30ns, CMOS PLD, Comm.	39-49

PRODUCT INDEX

PRODUCT DESIGNATION	DESCRIPTION	PAGES
CPL16V8-20NC	OTP, Plastic 20-pin, 1/2 Power, 20ns, CMOS PLD, Comm.	51-60
CPL16V8-20NLC	20-pin PLCC, 1/2 Power, 20ns, CMOS PLD, Comm.	51-60
CPL16V8L-25NC	OTP, Plastic 20-pin, 1/4 Power, 25ns, CMOS PLD, Comm.	51-60
CPL16V8L-25NLC	20-pin PLCC, 1/4 Power, 25ns, CMOS PLD, Comm.	51-60
CPL16V8L-25WC	20-pin Windowed CERDIP, 1/4 Power, 25ns, CMOS PLD, Comm.	51-60
CPL16V8-25NC	OTP, Plastic 20-pin, 1/2 Power, 25ns, CMOS PLD, Comm.	51-60
CPL16V8-25NLC	20-pin PLCC, 1/2 Power, 25ns, CMOS PLD, Comm.	51-60
CPL16V8L-30NC	OTP, Plastic 20-pin, 1/4 Power, 30ns, CMOS PLD, Comm.	51-60
CPL16V8L-30NLC	20-pin PLCC, 1/4 Power, 30ns, CMOS PLD, Comm.	51-60
CPL20V8-20NC	OTP, Plastic 24-pin, 1/2 Power, 20ns, CMOS PLD, Comm.	61-70
CPL20V8-20NLC	24-pin PLCC, 1/2 Power, 20ns, CMOS PLD, Comm.	61-70
CPL20V8L-25NC	OTP, Plastic 24-pin, 1/4 Power, 25ns, CMOS PLD, Comm.	61-70
CPL20V8L-25NLC	24-pin PLCC, 1/4 Power, 25ns, CMOS PLD, Comm.	61-70
CPL20V8L-25WC	24-pin Windowed CERDIP, 1/4 Power, 25ns, CMOS PLD, Comm.	61-70
CPL20V8-25NC	OTP, Plastic 24-pin, 1/2 Power, 25ns, CMOS PLD, Comm.	61-70
CPL20V8-25NLC	24-pin PLCC, 1/2 Power, 25ns, CMOS PLD, Comm.	61-70
CPL20V8L-30NC	OTP, Plastic 24-pin, 1/4 Power, 30ns, CMOS PLD, Comm.	61-70
CPL20V8L-30NLC	24-pin PLCC, 1/4 Power, 30ns, CMOS PLD, Comm.	61-70
CPL22V10L-25NC	OTP, Plastic 24-pin, 1/4 Power, 25ns, CMOS PLD, Comm.	71-78
CPL22V10L-25NLC	24-pin PLCC, 1/4 Power, 25ns, CMOS PLD, Comm.	71-78
CPL22V10L-25WC	24-pin Windowed CERDIP, 1/4 Power, 25ns, CMOS PLD, Comm.	71-78
CPL22V10-25NC	OTP, Plastic 24-pin, 1/2 Power, 25ns, CMOS PLD, Comm.	71-78
CPL22V10-25NLC	24-pin PLCC, 1/2 Power, 25ns, CMOS PLD, Comm.	71-78
CPL22V10L-35NC	OTP, Plastic 24-pin, 1/4 Power, 35ns, CMOS PLD, Comm.	71-78
CPL22V10L-35NLC	24-pin PLCC, 1/4 Power, 35ns, CMOS PLD, Comm.	71-78
CPL22V10-35NC	OTP, Plastic 24-pin, 1/2 Power, 35ns, CMOS PLD, Comm.	71-78
CPL22V10-35NLC	24-pin PLCC, 1/2 Power, 35ns, CMOS PLD, Comm.	71-78

PRODUCT SELECTION GUIDE

Part #	Pins	Array Inputs	Dedicated Inputs	I/O's	Outputs			Max Speed (ns) (1,2)					Max I_{CC} (mA)	
					Combinatorial	Registered	Total	-15[4]	-20	-25	-30	-35	Low Pwr.	Std. Pwr.
CPL16L8	20	16	10	6	8	0	8	t_{PD}=15	t_{PD}=20	t_{PD}=25	------	t_{PD}=35	35	70
CPL16R4	20	16	8	4	4	4	8	t_{PD}/t_{CO} =15/12	t_{PD}/t_{CO} =20/15	t_{PD}/t_{CO} =25/15	------	t_{PD}/t_{CO} =35/25	35	70
CPL16R6	20	16	8	2	2	6	8	t_{PD}/t_{CO} =15/12	t_{PD}/t_{CO} =20/15	t_{PD}/t_{CO} =25/15	------	t_{PD}/t_{CO} =35/25	35	70
CPL16R8	20	16	8	0	0	8	8	t_{CO}=12	t_{CO}=15	t_{CO}=15	------	t_{CO}=25	35	70
CPL20L8	24	20	14	6	8	0	8	t_{PD}=15	t_{PD}=20	t_{PD}=25	------	t_{PD}=35	35	70
CPL20R4	24	20	12	4	4	4	8	t_{PD}/t_{CO} =15/12	t_{PD}/t_{CO} =20/15	t_{PD}/t_{CO} =25/15	------	t_{PD}/t_{CO} =35/25	35	70
CPL20R6	24	20	12	2	2	6	8	t_{PD}/t_{CO} =15/12	t_{PD}/t_{CO} =20/15	t_{PD}/t_{CO} =25/15	------	t_{PD}/t_{CO} =35/25	35	70
CPL20R8	24	20	12	0	0	8	8	t_{CO}=15	t_{CO}=15	t_{CO}=15	------	t_{CO}=25	35	70
CPL20L10	24	20	12	8	10	0	10	t_{PD}=15	t_{PD}=20	t_{PD}=25	t_{PD}-30	------	35	70
CPL16V8[3]	20	16	10	8	Programmable Macrocell Outputs		8	------	t_{PD}/t_{CO} =25/15	t_{PD}/t_{CO} =25/15	$t_{PD}/t_{/CO}$ =30/20	------	45	70
CPL20V8[3]	24	20	14	8	Programmable Macrocell Outputs		8	------	t_{PD}/t_{CO} =25/15	t_{PD}/t_{CO} =25/15	$t_{PD}/t_{/CO}$ =30/20	------	45	70
CPL22V10[3]	24	22	12	10	Programmable Macrocell Outputs		10	------	------	t_{pd}/t_{co} =25/15	------	t_{pd}/t_{co} =35/25	55	90

Refer to the Product Index for the different packages that the devices are available in.

Notes:

(1) The above specifications are for the commercial temperature range of 0 to 70°C.
(2) Industrial product in the temperature range of -40°C to +105°C is also available.
(3) Contact factory for availability

CPL CROSS REFERENCE GUIDE

ATMEL PART #	SAMSUNG DESCRIPTION	SAMSUNG PART #
AT22V10	24-pin ½ Power, 25ns, Versatile CMOS PLD	CPL22V10-25
AMD/MMI		
PAL12L10	24-Pin ½ Power, 35ns, CMOS PLD	CPL20L10-30
PAL14L8	24-pin ½ Power, 35ns, CMOS PLD	CPL20L8-35
PAL16L6	24-pin ½ Power, 35ns, CMOS PLD	CPL20L8-35
PAL18L4	24-pin ½ Power, 35ns, CMOS PLD	CPL20L8-35
PAL16L8A	20-pin ½ Power, 25ns, CMOS PLD	CPL16L8-25
PAL16L8A-2	20-pin ½ Power, 35ns, CMOS PLD	CPL16L8-35
PAL16L8A-4	20-pin ¼ Power, 35ns, CMOS PLD	CPL16L8L-35
PAL16L8B	20-pin ½ Power, 15ns, CMOS PLD	CPL16L8-15
PAL16L8B-2	20-pin ½ Power, 25ns, CMOS PLD	CPL16L8-25
PAL16L8B-4	20-pin ¼ Power, 35ns, CMOS PLD	CPL16L8L-35
AmPAL16L8	20-pin ½ Power, 35ns, CMOS PLD	CPL16L8-35
AmPAL16L8L	20-pin ½ Power, 35ns, CMOS PLD	CPL16L8-35
AmPAL16L8Q	20-pin ¼ Power, 35ns, CMOS PLD	CPL16L8L-35
AmPAL16L8A	20-pin ½ Power, 25ns, CMOS PLD	CPL16L8-25
AmPAL16L8AL	20-pin ½ Power, 25ns, CMOS PLD	CPL16L8-25
AmPAL16L8B	20-pin ½ Power, 15ns, CMOS PLD	CPL16L8-15
PALC16L8Q-25	20-pin ¼ Power, 25ns, CMOS PLD	CPL16L8L-25
PAL16R4A	20-pin ½ Power, 25ns, CMOS PLD	CPL16R4-25
PAL16R4A-2	20-pin ½ Power, 35ns, CMOS PLD	CPL16R4-35
PAL16R4A-4	20-pin ¼ Power, 35ns, CMOS PLD	CPL16R4L-35
PAL16R4B	20-pin ½ Power, 15ns, CMOS PLD	CPL16R4-15
PAL16R4B-2	20-pin ½ Power, 25ns, CMOS PLD	CPL16R4-25
PAL16R4B-4	20-pin ¼ Power, 35ns, CMOS PLD	CPL16R4L-35
AmPAL16R4	20-pin ½ Power, 35ns, CMOS PLD	CPL16R4-35
AmPAL16R4L	20-pin ½ Power, 35ns, CMOS PLD	CPL16R4-35
AmPAL16R4Q	20-pin ¼ Power, 35ns, CMOS PLD	CPL16R4L-35
AmPAL16R4A	20-pin ½ Power, 25ns, CMOS PLD	CPL16R4-25
AmPAL16R4AL	20-pin ½ Power, 25ns, CMOS PLD	CPL16R4-25
AmPAL16R4B	20-pin ½ Power, 15ns, CMOS PLD	CPL16R4-15
PALC16R4Q-25	20-pin ½ Power, 25ns, CMOS PLD	CPL16R4L-25
PAL16R6A	20-pin ½ Power, 25ns, CMOS PLD	CPL16R6-25
PAL16R6A-2	20-pin ½ Power, 35ns, CMOS PLD	CPL16R6-35
PAL16R6A-4	20-pin ¼ Power, 35ns, CMOS PLD	CPL16R6L-35
PAL16R6B	20-pin ½ Power, 15ns, CMOS PLD	CPL16R6-15
PAL16R6B-2	20-pin ½ Power, 25ns, CMOS PLD	CPL16R6-25
PAL16R6B-4	20-pin ¼ Power, 35ns, CMOS PLD	CPL16R6L-35
AmPAL16R6	20-pin ½ Power, 35ns, CMOS PLD	CPL16R6-35
AmPAL16R6L	20-pin ½ Power, 35ns, CMOS PLD	CPL16R6-35
AmPAL16R6Q	20-pin ¼ Power, 35ns, CMOS PLD	CPL16R6L-35
AmPAL16R6A	20-pin ½ Power, 25ns, CMOS PLD	CPL16R6-25
AmPAL16R6AL	20-pin ½ Power, 25ns, CMOS PLD	CPL16R6-25
AmPAL16R6B	20-pin ½ Power, 15ns, CMOS PLD	CPL16R6-15

AMD/MMI PART #	DESCRIPTION	SAMSUNG PART #
PALC16R6Q-25	20-pin ¼ Power, 25ns, CMOS PLD	CPL16R6L-25
PAL16R8A	20-pin ½ Power, 25ns, CMOS PLD	CPL16R8-25
PAL16R8A-2	20-pin ½ Power, 35ns, CMOS PLD	CPL16R8-35
PAL16R8A-4	20-pin ¼ Power, 35ns, CMOS PLD	CPL16R8L-35
PAL16R8B	20-pin ½ Power, 15ns, CMOS PLD	CPL16R8-15
PAL16R8B-2	20-pin ½ Power, 25ns, CMOS PLD	CPL16R8-25
PAL16R8B-4	20-pin ¼ Power, 35ns, CMOS PLD	CPL16R8L-35
AmPAL16R8	20-pin ½ Power, 35ns, CMOS PLD	CPL16R8-35
AmPAL16R8L	20-pin ½ Power, 35ns, CMOS PLD	CPL16R8-35
AmPAL16R8Q	20-pin ¼ Power, 35ns, CMOS PLD	CPL16R8L-35
AmPAL16R8A	20-pin ½ Power, 25ns, CMOS PLD	CPL16R8-25
AmPAL16R8AL	20-pin ½ Power, 25ns, CMOS PLD	CPL16R8-25
AmPAL16R8B	20-pin ½ Power, 15ns, CMOS PLD	CPL16R8-15
PALC16R8Q-25	20-pin ¼ Power, 25ns, CMOS PLD	CPL16R8L-25
PAL20L10A	24-pin ½ Power, 25ns, CMOS PLD	CPL20L10-25
AmPAL20L10AL	24-pin ½ Power, 25ns, CMOS PLD	CPL20L10-25
AmPAL20L10B	24-pin ½ Power, 15ns, CMOS PLD	CPL20L10-15
AmPAL20L10-20	24-pin ½ Power, 20ns, CMOS PLD	CPL20L10-20
PAL20L8A	24-pin ½ Power, 25ns, CMOS PLD	CPL20L8-25
PAL20L8A-2	24-pin ½ Power, 35ns, CMOS PLD	CPL20L8-35
PAL20L8B	24-pin ½ Power, 15ns, CMOS PLD	CPL20L8-15
PAL20L8B-2	24-pin ½ Power, 25ns, CMOS PLD	CPL20L8-25
PAL20R4A	24-pin ½ Power, 25ns, CMOS PLD	CPL20R4-25
PAL20R4A-2	24-pin ½ Power, 35ns, CMOS PLD	CPL20R4-35
PAL20R4B	24-pin ½ Power, 15ns, CMOS PLD	CPL20R4-15
PAL20R4B-2	24-pin ½ Power, 25ns, CMOS PLD	CPL20R4-25
PAL20R6A	24-pin ½ Power, 25ns, CMOS PLD	CPL20R6-25
PAL20R6A-2	24-pin ½ Power, 35ns, CMOS PLD	CPL20R6-35
PAL20R6B	24-pin ½ Power, 35ns, CMOS PLD	CPL20R6-15
PAL20R6B-2	24-pin ½ Power, 25ns, CMOS PLD	CPL20R6-25
PAL20R8A	24-pin ½ Power, 25ns, CMOS PLD	CPL20R8-25
PAL20R8A-2	24-pin ½ Power, 35ns, CMOS PLD	CPL20R8-35
PAL20R8B	24-pin ½ Power, 15ns, CMOS PLD	CPL20R8-15
PAL20R8B-2	24-pin ½ Power, 25ns, CMOS PLD	CPL20R8-25
PALC22V10H-25	24-pin ½ Power, 25ns, Versatile CMOS PLD	CPL22V10-25
PALC22V10H-35	24-pin ½ Power, 35ns, Versatile CMOS PLD	CPL22V10-35
AmPAL22V10	24-pin ½ Power, 35ns, Versatile CMOS PLD	CPL22V10-35
AmPAL22V10A	24-pin ½ Power, 25ns, Versatile CMOS PLD	CPL22V10-25

CPL CROSS REFERENCE GUIDE (Continued)

CYPRESS PART #	SAMSUNG DESCRIPTION	SAMSUNG PART #
PALC16L8-15	20-pin ½ Power, 15ns, CMOS PLD	CPL16L8-15
PALC16L8L-15	20-pin ¼ Power, 15ns, CMOS PLD	CPL16L8L-15
PALC16L8-25	20-pin ½ Power, 25ns, CMOS PLD	CPL16L8-25
PALC16L8L-25	20-pin ¼ Power, 25ns, CMOS PLD	CPL16L8L-25
PALC16L8-35	20-pin ½ Power, 35ns, CMOS PLD	CPL16L8-35
PALC16L8L-35	20-pin ¼ Power, 35ns, CMOS PLD	CPL16L8L-35
PALC16R4-15	20-pin ½ Power, 15ns, CMOS PLD	CPL16R4-15
PALC16R4L-15	20-pin ¼ Power, 15ns, CMOS PLD	CPL16R4L-15
PALC16R4-25	20-pin ½ Power, 25ns, CMOS PLD	CPL16R4-25
PALC16R4L-25	20-pin ¼ Power, 25ns, CMOS PLD	CPL16R4L-25
PALC16R4-35	20-pin ½ Power, 35ns, CMOS PLD	CPL16R4-35
PALC16R4L-35	20-pin ¼ Power, 35ns, CMOS PLD	CPL16R4L-35
PALC16R6-15	20-pin ½ Power, 15ns, CMOS PLD	CPL16R6-15
PALC16R6L-15	20-pin ¼ Power, 15ns, CMOS PLD	CPL16R6L-15
PALC16R6-25	20-pin ½ Power, 25ns, CMOS PLD	CPL16R6-25
PALC16R6L-25	20-pin ¼ Power, 25ns, CMOS PLD	CPL16R6L-25
PALC16R6-35	20-pin ½ Power, 35ns, CMOS PLD	CPL16R6-35
PALC16R6L-35	20-pin ¼ Power, 35ns, CMOS PLD	CPL16R6L-35
PALC16R8-15	20-pin ½ Power, 15ns, CMOS PLD	CPL16R8-15
PALC16R8L-15	20-pin ¼ Power, 15ns, CMOS PLD	CPL16R8L-15
PALC16R8-25	20-pin ½ Power, 25ns, CMOS PLD	CPL16R8-25
PALC16R8L-25	20-pin ¼ Power, 25ns, CMOS PLD	CPL16R8L-25
PALC16R8-35	20-pin ½ Power, 35ns, CMOS PLD	CPL16R8-35
PALC16R8L-35	20-pin ¼ Power, 35ns, CMOS PLD	CPL16R8L-35
PALC22V10-25	24-pin ½ Power, 25ns, Versatile CMOS PLD	CPL22V10-25
PALC22V10L-25	24-pin ¼ Power, 25ns, Versatile CMOS PLD	CPL22V10L-25
PALC22V10-35	24-pin ½ Power, 35ns, Versatile CMOS PLD	CPL22V10-35
PALC22V10L-35	24-pin ¼ Power, 35ns, Versatile CMOS PLD	CPL22V10L-35
GOULD		
22CV10-25	24-pin ½ Power, 25ns, Versatile CMOS PLD	CPL22V10-25
22CV10-35	24-pin ½ Power, 35ns, Versatile CMOS PLD	CPL22V10-35
HARRIS		
HPL16LC8-5*	20-pin ¼ Power, 35ns, CMOS PLD	CPL16L8L-35
HPL16RC4-5*	20-pin ¼ Power, 35ns, CMOS PLD	CPL16R4L-35
HPL16RC6-5*	20-pin ¼ Power, 35ns, CMOS PLD	CPL16R6L-35
HPL16RC8-5*	20-pin ¼ Power, 35ns, CMOS PLD	CPL16R8L-35
ICT		
PEEL22CV10-25	24-pin ½ Power, 25ns, Versatile CMOS PLD	CPL22V10-25
PEEL22CV10-30	24-pin ½ Power, 25ns, Versatile CMOS PLD	CPL22V10-25
PEEL22CV10-35	24-pin ½ Power, 35ns, Versatile CMOS PLD	CPL22V10-35

LATTICE PART #	SAMSUNG DESCRIPTION	SAMSUNG PART #
GAL16V8-20L	20-pin ½ Power, 20ns, CMOS PLD Superset	CPL16V8-20
GAL16V8-25Q	20-pin ¼ Power, 25ns, CMOS PLD Superset	CPL16V8L-25
GAL16V8-25L	20-pin ½ Power, 25ns, CMOS PLD Superset	CPL16V8-25
GAL16V8-30Q	20-pin ¼ Power, 30ns, CMOS PLD Superset	CPL16V8L-30
GAL20V8-20L	24-pin ½ Power, 20ns CMOS PLD Superset	CPL20V8-20
GAL20V8-25Q	24-pin ¼ Power, 25ns CMOS PLD Superset	CPL20V8L-25
GAL20V8-25L	24-pin ½ Power, 25ns CMOS PLD Superset	CPL20V8-25
GAL20V8-30Q	24-pin ¼ Power, 30ns CMOS PLD Superset	CPL20V8L-30
NATIONAL		
PAL16L8	20-pin ½ Power, 35ns, CMOS PLD	CPL16L8-35
PAL16L8A	20-pin ½ Power, 25ns, CMOS PLD	CPL16L8-25
PAL16L8A2	20-pin ½ Power, 35ns, CMOS PLD	CPL16L8-35
PAL16L8B	20-pin ½ Power, 15ns, CMOS PLD	CPL16L8-15
PAL16L8B2	20-pin ½ Power, 25ns, CMOS PLD	CPL16L8-25
PAL16R4	20-pin ½ Power, 35ns, CMOS PLD	CPL16R4-35
PAL16R4A	20-pin ½ Power, 25ns, CMOS PLD	CPL16R4-25
PAL16R4A2	20-pin ½ Power, 35ns, CMOS PLD	CPL16R4-35
PAL16R4B	20-pin ½ Power, 15ns, CMOS PLD	CPL16R4-15
PAL16R4B2	20-pin ½ Power, 25ns, CMOS PLD	CPL16R4-25
PAL16R6	20-pin ½ Power, 35ns, CMOS PLD	CPL16R6-35
PAL16R6A	20-pin ½ Power, 25ns, CMOS PLD	CPL16R6-25
PAL16R6A2	20-pin ½ Power, 35ns, CMOS PLD	CPL16R6-35
PAL16R6B	20-pin ½ Power, 15ns, CMOS PLD	CPL16R6-15
PAL16R6B2	20-pin ½ Power, 25ns, CMOS PLD	CPL16R6-25
PAL16R8	20-pin ½ Power, 35ns, CMOS PLD	CPL16R8-35
PAL16R8A	20-pin ½ Power, 25ns, CMOS PLD	CPL16R8-25
PAL16R8A2	20-pin ½ Power, 35ns, CMOS PLD	CPL16R8-35
PAL16R8B	20-pin ½ Power, 15ns, CMOS PLD	CPL16R8-15
PAL16R8B2	20-pin ½ Power, 25ns, CMOS PLD	CPL16R8-25
PAL20L8A	24-pin ½ Power, 25ns, CMOS PLD	CPL20L8-25
PAL20L8B	24-pin ½ Power, 15ns, CMOS PLD	CPL20L8-15
PAL20R4A	24-pin ½ Power, 25ns, CMOS PLD	CPL20R4-25
PAL20R4B	24-pin ½ Power, 15ns, CMOS PLD	CPL20R4-15
PAL20R6A	24-pin ½ Power, 25ns, CMOS PLD	CPL20R6-25
PAL20R6B	24-pin ½ Power, 15ns, CMOS PLD	CPL20R6-15
PAL20R8A	24-pin ½ Power, 25ns, CMOS PLD	CPL20R8-25
PAL20R8B	24-pin ½ Power, 15ns, CMOS PLD	CPL20R8-15
PAL12L10	24-pin ½ Power, 35ns, CMOS PLD	CPL20L10-30
PAL14L8	24-pin ½ Power, 35ns, CMOS PLD	CPL20L8-35
PAL16L6	24-pin ½ Power, 35ns, CMOS PLD	CPL20L8-35
PAL18L4	24-pin ½ Power, 35ns, CMOS PLD	CPL20L8-35

* These devices have programmable polarity outputs. Please check output polarity for crossing accuracy.

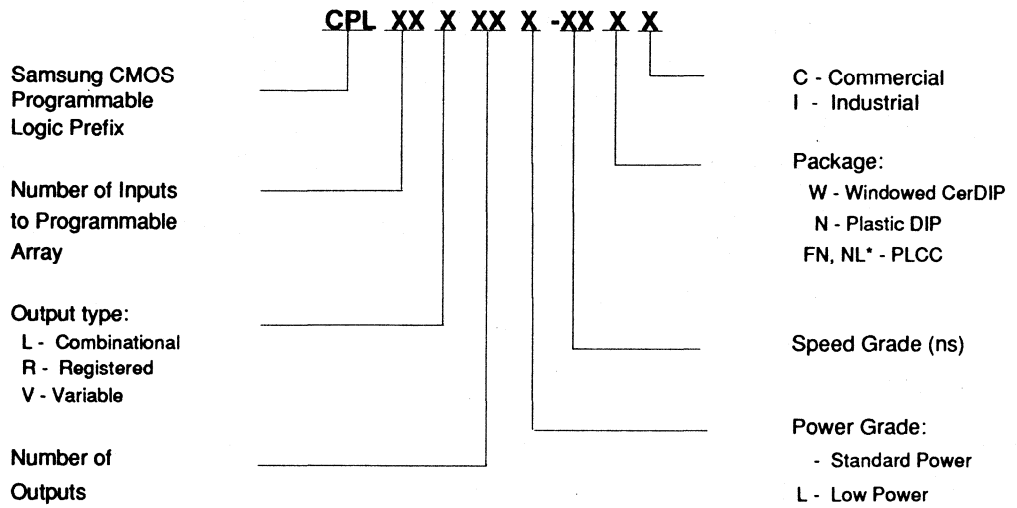
CPL CROSS REFERENCE GUIDE (Continued)

NATIONAL PART #	SAMSUNG DESCRIPTION	SAMSUNG PART #
PAL12L10A	24-pin ½ Power, 25ns, CMOS PLD	CPL20L10-25
PAL14L8A	24-pin ½ Power, 25ns, CMOS PLD	CPL20L8-25
PAL16L6A	24-pin ½ Power, 25ns, CMOS PLD	CPL20L8-25
PAL18L4A	24-pin ½ Power, 25ns, CMOS PLD	CPL20L8-25
PAL20L10	24-pin ½ Power, 35ns, CMOS PLD	CPL20L10-30
PAL20L10A	24-pin ½ Power, 25ns, CMOS PLD	CPL20L10-25
GAL16V8-20L	20-pin ½ Power, 20ns, CMOS PLD Superset	CPL16V8-20
GAL16V8-25Q	20-pin ¼ Power, 25ns, CMOS PLD Superset	CPL16V8L-25
GAL16V8-25L	20-pin ½ Power, 25ns, CMOS PLD Superset	CPL16V8-25
GAL16V8-30Q	20-pin ¼ Power, 30ns, CMOS PLD Superset	CPL16V8L-30
GAL20V8-20L	24-pin ½ Power, 20ns CMOS PLD Superset	CPL20V8-20
GAL20V8-25Q	24-pin ¼ Power, 25ns CMOS PLD Superset	CPL20V8L-25
GAL20V8-25L	24-pin ½ Power, 25ns CMOS PLD Superset	CPL20V8-25
GAL20V8-30Q	24-pin ¼ Power, 30ns CMOS PLD Superset	CPL20V8L-30
SIGNETICS		
PLHS16L8A	20-pin ½ Power, 20ns, CMOS PLD	CPL16L8-20
PLHS16L8B	20-pin ½ Power, 15ns, CMOS PLD	CPL16L8-15
PLC16V8-35Q	20-pin ¼ Power, 35ns, CMOS PLD Superset	CPL16V8L-30
PLC16V8-35H	20-pin ½ Power, 35ns, CMOS PLD Superset	CPL16V8-30
PLC20V8-35Q	24-pin ¼ Power, 35ns, CMOS PLD Superset	CPL20V8L-30
PLC20V8-35H	24-pin ½ Power, 35ns, CMOS PLD Superset	CPL20V8-30
SGS		
GAL16V8-20L	20-pin ½ Power, 20ns, CMOS PLD Superset	CPL16V8-20
GAL16V8-25Q	20-pin ¼ Power, 25ns, CMOS PLD Superset	CPL16V8L-25
GAL16V8-25L	20-pin ½ Power, 25ns, CMOS PLD Superset	CPL16V8-25
GAL16V8-30Q	20-pin ¼ Power, 30ns, CMOS PLD Superset	CPL16V8L-30
GAL20V8-20L	24-pin ½ Power, 20ns CMOS PLD Superset	CPL20V8-20
GAL20V8-25Q	24-pin ¼ Power, 25ns CMOS PLD Superset	CPL20V8L-25
GAL20V8-25L	24-pin ½ Power, 25ns CMOS PLD Superset	CPL20V8-25
GAL20V8-30Q	24-pin ¼ Power, 30ns CMOS PLD Superset	CPL20V8L-30

TI PART #	SAMSUNG DESCRIPTION	SAMSUNG PART #
PAL16L8A	20-pin ½ Power, 25ns, CMOS PLD	CPL16L8-25
PAL16L8A-2	20-pin ½ Power, 35ns, CMOS PLD	CPL16L8-35
TIB PAL16L8-15	20-pin ½ Power, 15ns, CMOS PLD	CPL16L8-15
TIB PAL16L8-25	20-pin ½ Power, 25ns, CMOS PLD	CPL16L8-25
PAL16R4A	20-pin ½ Power, 25ns, CMOS PLD	CPL16R4-25
PAL16R4A-2	20-pin ½ Power, 35ns, CMOS PLD	CPL16R4-35
TIB PAL16R4-15	20-pin ½ Power, 15ns, CMOS PLD	CPL16R4-15
TIB PAL16R4-25	20-pin ½ Power, 25ns, CMOS PLD	CPL16R4-25
PAL16R6A	20-pin ½ Power, 25ns, CMOS PLD	CPL16R6-25
PAL16R6A-2	20-pin ½ Power, 35ns, CMOS PLD	CPL16R6-35
TIB PAL16R6-15	20-pin ½ Power, 15ns, CMOS PLD	CPL16R6-15
TIB PAL16R6-25	20-pin ½ Power, 25ns, CMOS PLD	CPL16R6-25
PAL16R8A	20-pin ½ Power, 25ns, CMOS PLD	CPL16R8-25
PAL16R8A-2	20-pin ½ Power, 35ns, CMOS PLD	CPL16R8-35
TIB PAL16R8-15	20-pin ½ Power, 15ns, CMOS PLD	CPL16R8-15
TIB PAL16R8-25	20-pin ½ Power, 25ns, CMOS PLD	CPL16R8-25
PAL20L8A	24-pin ½ Power, 25ns, CMOS PLD	CPL20L8-25
TIB PAL20L8-15	24-pin ½ Power, 15ns, CMOS PLD	CPL20L8-15
TIB PAL20L8-25	24-pin ½ Power, 25ns, CMOS PLD	CPL20L8-25
PAL20R4A	24-pin ½ Power, 25ns, CMOS PLD	CPL20R4-25
TIB PAL20R4-15	24-pin ½ Power, 15ns, CMOS PLD	CPL20R4-15
TIB PAL20R4-25	24-pin ½ Power, 25ns, CMOS PLD	CPL20R4-25
PAL20R6A	24-pin ½ Power, 25ns, CMOS PLD	CPL20R6-25
TIB PAL20R6-15	24-pin ½ Power, 15ns, CMOS PLD	CPL20R6-15
TIB PAL20R6-25	24-pin ½ Power, 25ns, CMOS PLD	CPL20R6-25
PAL20R8A	24-pin ½ Power, 25ns, CMOS PLD	CPL20R8-25
TIB PAL20R8-15	24-pin ½ Power, 15ns, CMOS PLD	CPL20R8-15
TIB PAL20R8-25	24-pin ½ Power, 25ns, CMOS PLD	CPL20R8-25
TIB PAL20L10-20	24-pin ½ Power, 15ns, CMOS PLD	CPL20L10-20
TIB PAL20L10-30	24-pin ½ Power, 25ns, CMOS PLD	CPL20L10-25
TIB PAL22V10	24-pin ½ Power, 35ns Versatile CMOS PLD	CPL22V10-35
TIB PAL22V10A	24-pin ½ Power, 25ns Versatile CMOS PLD	CPL22V10-25

1

CPL™ ORDERING INFORMATION



*For JEDEC PLCC availability, please contact factory

Product Guide 1

Technical Overview/Quality and Reliability 2

Product Specifications 3

CPL Programming Electrical Specifications 4

CPL Starter Kit/CPL Programmer and Software Guide 5

Definition of Terms 6

Package Drawings 7

Sales Offices 8

Samsung CPL Family Features

Samsung's CPL (CMOS Programmable Logic) devices use a state-of-the-art CMOS EPROM technology which emphasizes complete testability. The 1.2 micron advanced CMOS process provides high performance, which was previously achieved only with bipolar processes, at a much lower power. Testability is inherent to the technology because it allows devices to be programmed and erased, thus facilitating 100% programming, AC, and functional testing.

The first generation of CPL devices are CMOS implementations of the industry standard PAL devices. The CPL devices offer significant advantages over TTL logic, some of which are listed below:

- 100% user-programmability
- Design flexibility
- Chip-count and pin-count reduction
- Pattern duplication prevention (Security Bit)

The CPL family also offers additional features and benefits which can be attributed to the CMOS EPROM technology:

- 100% programming, AC and, functional testing
- Increased reliabiltiy
- Easier, lower-cost prototyping with reprogrammable CPL devices (windowed, CERDIP)
- Lower power consumption over bipolar PALs with matched performance

The CPL EPROM cells are programmed by charging a floating gate with electrons and unprogrammed by irradiating the cells with ultraviolet (UV) light, making complete testing of all circuitry possible before shipping. On the other hand, bipolar devices which use fuse programmable cells, can be programmed only once, making 100% testing impossible. Special, on-chip test arrays also allow additional functional and AC testing without having to program the CPL devices.

CPL devices which are contained in windowed CERDIP packages may be programmed and erased, at the customer site. This allows the designer to develop, test, and fine-tune his/her logic without having to replace each programmed device.

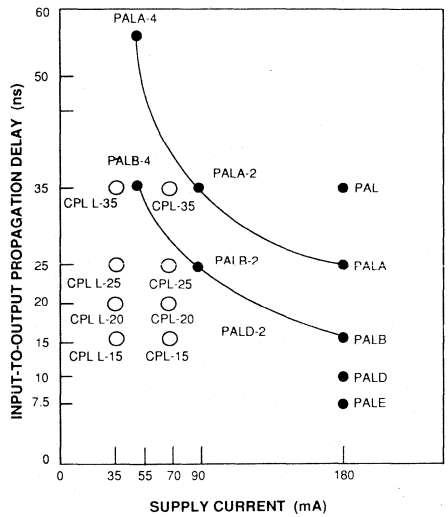
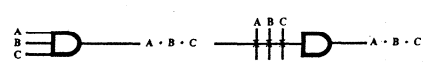


Figure 1. CPL-PAL Comparison

The CPL family offers the system designer a better alternative to the standard bipolar PLDs (Programmable Logic Devices). The devices are function and pinout compatible with their respective PAL predecessors. They may be designed into existing PAL sockets without changing the board layout or the PLD equations. The propagation delays of the CPL devices are 25 nsec or 35 nsec with 45mA or 70mA (max.) I_{CC}. Thus, the CPL devices provide bipolar speeds at a fraction of the bipolar power consumption, reducing the system's power requirements and increasing its reliability.

PLD Notation

In describing CPL devices, an industry standard PLD notation is used. Figure 2a shows the conventional notation of a multiple-input AND gate. Figure 2b shows the adopted PLD notation of the same logic gate. An X on an intersection of an input term and the input line of an AND gate represents that the input term is connected



a. **b.**

Figure 2. PLD Notation Example

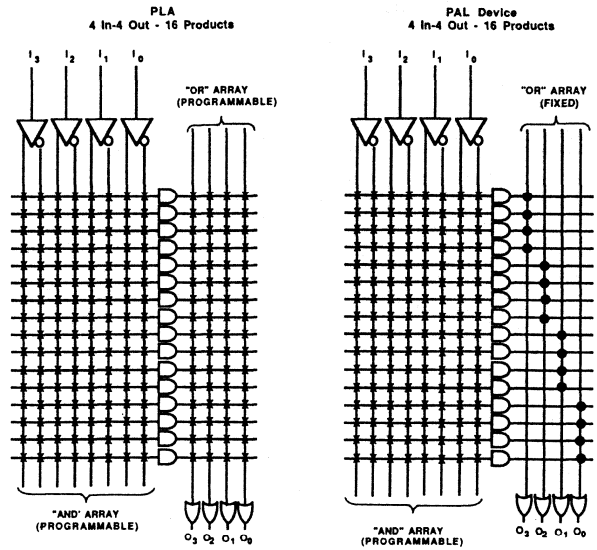


Figure 3. PLA and PAL AND-OR Structure

to one of the AND gate inputs. In a physical CPL device, an X represents an unprogrammed cell. (In an unprogrammed CPL device, all input terms are connected to all AND gates.) Each CPL device is illustrated by a logic diagram similar to the basic AND-OR structure diagram shown in Figure 3.

CPL Architecture

The CPL devices utilize the basic PLA (Programmable Logic Array) structure. This structure consists of an AND array followed by an OR array (see Figure 3). The CPL devices, like the PAL devices which they may replace, have a programmable AND array followed by a non-programmable OR array. Such a structure offers PLA flexibility while decreasing silicon complexity. In comparison, an FPLA (Field Programmable Logic Array) structure has both arrays programmable but occupies more silicon area.

The CPL devices, which have a basic PLA structure, lend themselves to easy implementation of Boolean

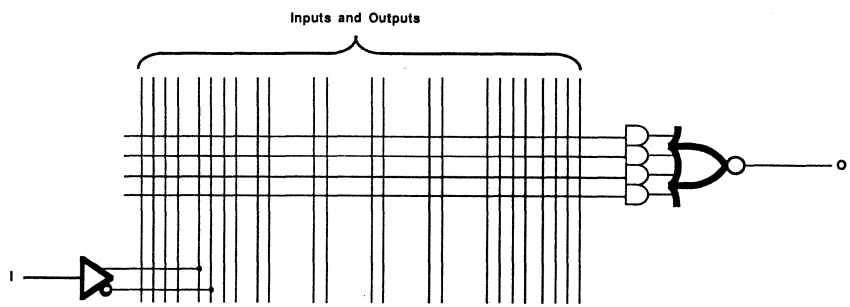


Figure 4. A Simple Combinatorial Output Structure

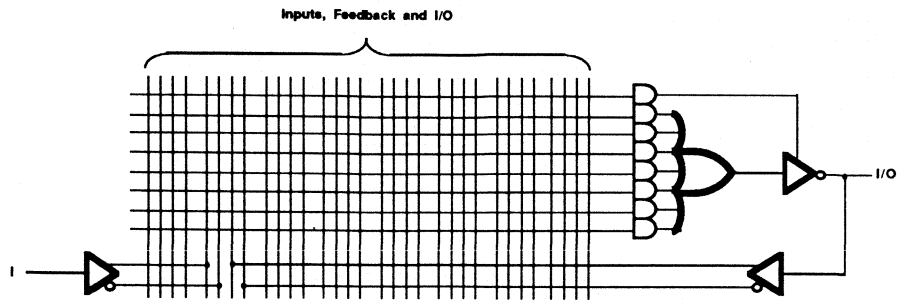


Figure 5. The Programmable Combinatorial Input/Output Structure

transfer functions. These functions are expressed in the sum-of-products form. This allows quick and easy implementation of logic functions of varying complexity.

The CPL devices allow the designer to configure complex interconnections within the chip as opposed to configuring them on the PC board. The design, therefore, becomes more efficient and takes less time to complete. Furthermore, the interconnections, made by writing into EPROM cells, can be easily modified during prototype testing, saving lengthy and costly printed circuit board changes.

One CPL device can implement logic functions that require four or more conventional logic packages, reducing IC inventories while increasing board savings.

While all CPL devices are based on the PLA structure, they differ in their output structure combinations. The CPL devices feature a variety of output structures: combinatorial outputs, registered outputs, and programmable macro cells.

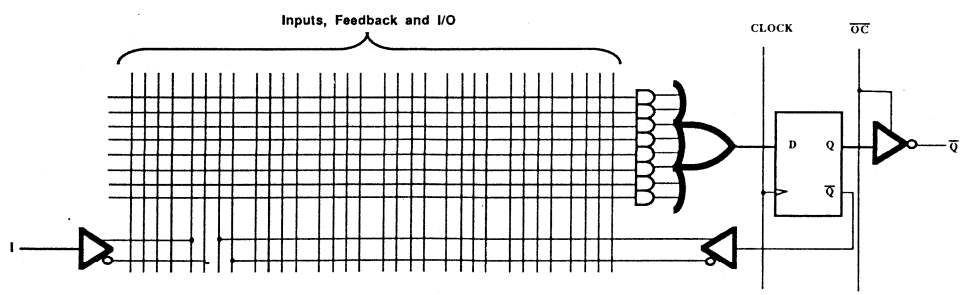


Figure 6. A Registered Output Structure with Feedback

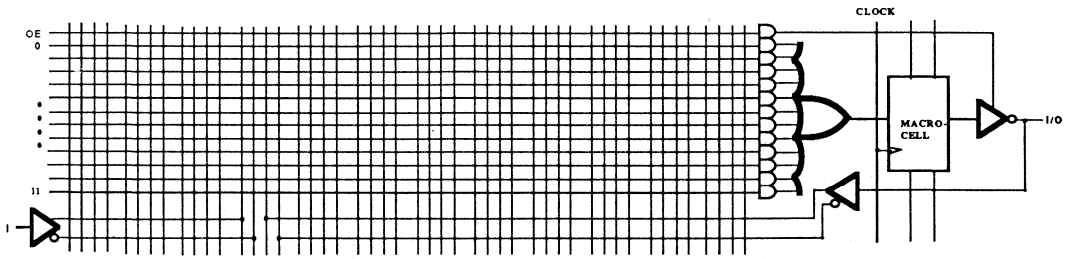


Figure 7. A Programmable Macro Cell Output Structure

Combinatorial Outputs

There are two types of combinatorial outputs. The simplest one is a combinatorial output without feedback (see Figure 4). It is used in the CPL16L8, CPL20L8, and CPL20L10 devices. This output sums several product terms (P-terms) into an active low signal. One additional P-term is used to individually enable/disable the output signal.

Another type of combinatorial output is the programmable combinatorial I/O (see Figure 5). When enabled, this output stage acts like the simple combinatorial output with the addition of a feedback path into the AND array. When disabled, the output stage allows the I/O pin to act as an input into the CPL AND array. This flexibility allows variable input/output ratios as well as bidirectional parts. The programmable combinatorial I/O output is used in all CPL20 and CPL24 devices with the exception of the CPL16R8 and CPL20R8.

Registered Outputs

This type of output features a data register with registered feedback. Each product term is summed into the data input of a D-type flip-flop. The flip-flop records the state of its input on the rising edge of the clock. The Q output of the flip-flop is gated to the output pin through a three-state buffer and is also fed back to the CPL AND array as an input term. This feature allows the CPL device to implement a state machine. The Clock and Output Enable/Disable signals are common to all registered outputs of a single device (See Figure 6). Registered outputs are used in all CPL20 and CPL24 devices with the exception of CPL16L8, CPL20L8, and CPL20L10.

Programmable Macro Cell I/O

The programmable macro cell, illustrated in Figure 7, is a very flexible structure which allows the designer to individually define the architecture of each I/O. Each I/O structure may be configured to be a combinatorial or registered output. Each output features an individually programmable Output Enable/Disable function as well as an individually programmable polarity function. Common Clock, Reset, and Preset signals facilitate preload, power reset and state-machine operations. Programmable macro cells are used in the CPL16V8 and CPL22V10 devices.

Test Circuitry

A PLD is tested, like any other digital circuit, by applying known values to its inputs. A fault may be detected by comparing the device's outputs with desired values. In general, a non-programmed PLD does not lend itself to exhaustive fault testing. Furthermore, since some of the PLDs have registered outputs with internal feedback lines to the programmable array, these feedback lines must be controlled during testing as well. Applying known values at these inputs of the array requires the application of many vectors to the device's inputs. Therefore, the device must be cycled many times to arrive at a known state, and the testing of the device becomes long and impractical.

To solve this problem, Samsung's CPL incorporates register preload and test arrays onto the devices, making testing simple and complete.

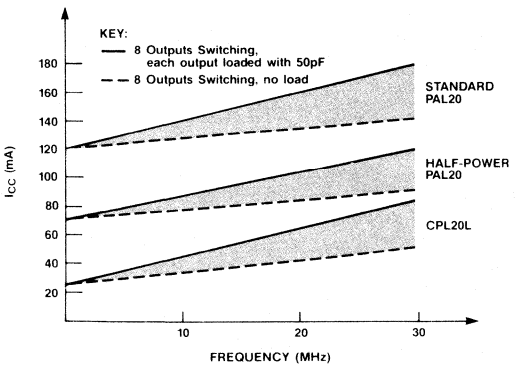


Figure 8. CPL and PAL Power Consumption as a Function of Frequency

Register Preload

The register preload feature allows the user, as well as the manufacturer, to load known values into the device's output registers. Known values are then applied to the array's feedback lines to help facilitate simple and complete device testing. The register preload operation is accomplished by applying a super-voltage pulse to a specified pin (see data sheets).

Test Array

The on-chip test array consists of additional input termswhich may be accessed for AC and functional testing before and after packaging. The test array is not accessed during, and does not affect, normal device operation. During testing, the test array is activated and used to drive the device circuitry, bypassing the non-programmed programmable array. The test array is used during in-house final testing and may also be used by the customer for incoming inspection.

CPL Development Software

A variety of software packages are available to define and simulate CPL devices. All CPL devices are supported by industry-standard software packages such as Data I/O's ABEL, P-CAD's CUPL, and others. These software packages assemble CPL definition files in various formats, simulate the CPL devices, and create bit patterns conforming to a JEDEC standard format that may be transmitted to PLD programming systems.

The CPL devices can be programmed by all major PROM/PLD systems. Some PROM/PLD programmers may require a software update or a personality card/module to facilitate CPL programming. All programmers accept bit patterns which conform to JEDEC standard format.

More detailed information and a list of PLD software vendors and programmers is included in the CPL Programmer and Software Guide section of this book.

Power Dissipation

Low power consumption is one of the most important features of CMOS technology. With most of the power dissipating only during device switching, it is important to describe the power dissipation in terms which reflect its dependency on operating frequency.

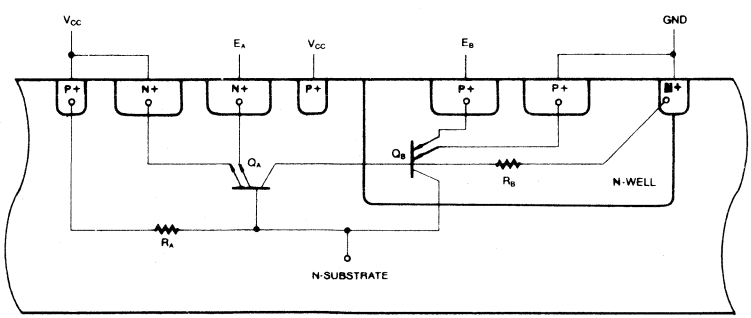


Figure 9. Simplified Cross Section of a CMOS Inverter

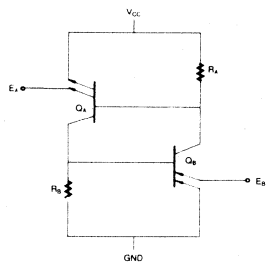


Figure 10. CMOS SCR Structure

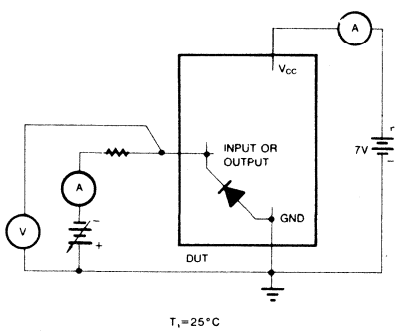


Figure 11. Test Setup for Measuring DC Latch-Up

A standard power dissipation model includes the device's quiescent current (I_Q), the device's internal "power dissipation" capacitance (C_{PD}), the external load capacitance (C_L), and the output buffer capacitance (C_O):

$$P_D = V_{CC}I_Q + C_{PD}V_{CC}^2f + (C_L+C_O)V_{DS}^2f$$

The quiescent power is determined by the static current. The switching power consumption is determined by the internal power dissipation capacitance and by the operating frequency (f). The power consumed by driving the external load depends on the external load itself, the output buffer capacitance, the operating frequency (f), and the output low-to-high voltage swing (V_{DS}).

The internal power capacitance as well as the static supply current vary from one CPL type to another. Moreover, they depend on the specific code which is programmed into the device. The typical I_Q for CPL20 and CPL24 is 25mA, and the typical C_{PD} is 45pF. The load capacitance plays an even more important role in determining the power consumption of a CPL device. Since 8 outputs may toggle, each consisting of typically 10pF, and each driving a 50pF load, up to 2.4 mA per MHz may add to the device's static supply current.

The graph in Figure 8 illustrates CPL power consumption as a function of operating frequency in comparison with bipolar PAL power consumption. All unused inputs are assumed to be tied to ground or V_{CC}, all active inputs are driven rail-to-rail, and the duty cycle is 50%. Measurements have shown that while the duty cycle does not greatly affect the CPL power consumption, up to 20% more power is consumed by the input buffers when the input voltage swings between 0.8V to 2.0V.

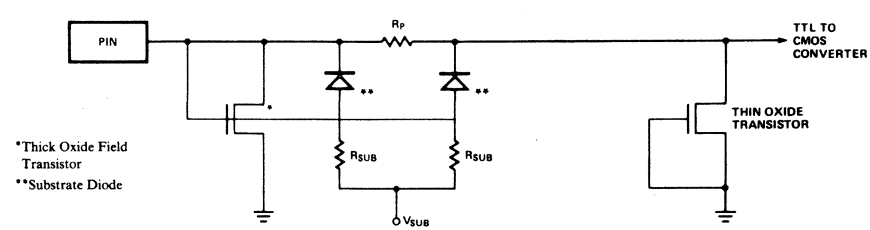


Figure 12. Input Protection Circuit

Latchup

In circuits fabricated using CMOS technology, a parasitic four- layer SCR structure appears between V_{CC} and ground. This parasitic structure can short V_{CC} to ground when voltages greater than V_{CC} or lower than ground are applied to an input or an output pin. The phenomenon is called "*latchup*" and may result in a damaged device. When a device is in latchup mode, the power supply must be shut-off to release the device back to normal operating mode.

The parasitic SCR structure in CMOS is illustrated in the simplified cross section of an inverter shown in Figure 9. Figure 10 shows a schematic representation of the same structure. When EA is raised above V_{CC}, current is injected from the emitter of QA and is swept to its collector. This current will increase the voltage at the gate of QB and once above 0.78V, it will turn QB on. QB will feed current back into RA and once a 0.7V voltage drop appears across RA, QA will turn on and inject more current into RB. Once both transistors are on and enough current is provided to sustain the SCR, it will stay on even after EA and EB return to within the rail voltages.

Because low RA and RB resistance values reduce the gain of QA and QB, Samsung's CPL devices are designed to have low RA and RB. In addition, large diodes are connected between each signal pin and the supply, to shunt out latchup trigger currents.

When a p-channel MOS transistor is used as a pull-up transistor on the output driver of an IC, another parasitic transistor is formed which worsens the latchup problem. The CPL devices use N- channel pull-up transistors which maintain TTL compatibility and improve latchup protection.

A substrate bias generator provides important additional latchup protection in CPL devices. It keeps the substrate at approximately -3V below ground level. The parasitic diode at an input pin will not turn on unless the voltage applied to that pin is more negative than -3V. The substrate bias also eliminates the substrate currents due to undershoot, thereby providing higher input noise tolerance.

Samsung's CPL devices are designed to withstand currents typically well above the specified minimum of 200 mA at 7V V_{CC} and 125°C. This parameter is measured on a static basis (see Figure 11).

ESD Protection

ESD protection is accomplished by preventing a high voltage from reaching the internal transistors of the integrated circuit. The circuit of each input pin includes a thick-oxide transistor, a thin-oxide transistor and the line resistance, Rp, between the transistors (see Figure 12). The thick-oxide transistor turns on when a large positive voltage is applied to the input pin. When the voltage arriving at the thin-oxide transistor exceeds 13V, the transistor turns on and protects the internal circuitry by discharging the current to ground. This current is then limited by the line resistance, Rp. A high negative voltage applied to the input pin is similarly discharged by the network of the substrate diodes which start conducting when the applied negative voltage is below the substrate level. The ESD protection incorporated in the output structure is shown in Figure 13. All CPL devices are protected with up to 2000V ESD protection.

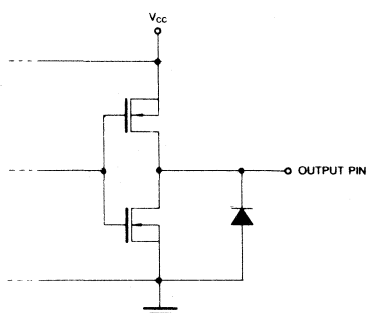


Figure 13. A typical output circuit of a CPL device.

CPL Quality and Reliability Program

Samsung has established a comprehensive reliability program to monitor and ensure the ongoing reliability of the high-performance CPL (CMOS Programmalbe Logic) family. This program entails rigorous on-line quality control as well as the collection and analysis of reliability data to meet Samsung's stringent quality standards.

At wafer sort 1, all CPL dies are programmed and tested for electrical parameters. In order to check the staying power of programmed data (called "charge retention"), each wafer is baked at 250°C for 168 hours. At wafer sort 2, the data is verified for retention, and subsequently erased in preparation for more tests. Only CPL devices that pass these wafer tests are assembled, ensuring 100-percent programmability.

After the CPL devices are assembled, they undergo complete DC testing again. An on-chip test array is also used to test the devices for full funtionality as well as for meeting all AC timing specifications. These tests are performed before and after production burn-in. This is followed by visual and mechanical inspection of each device. A production sample is also subjected to infant life testing and Data I/O programmability tests.

The tests run by the Quality and Reliability Department are accelerated tests, that serve to model "real world" applications through boosted temperatures, voltages and humidities. MIL-STD-883 and JEDEC standard methods and reliability procedures are used in testing. The following are summaries of various stresses and conditions that CPL devices are subjected to:

High Temperature Dynamic Operating Life Test (5.5V, 125°C)
The High Temperature Dynamic Operating Life Test is used to accelerate failure mechanisms by operating the devices at an elevated temperature. The data obtained by this life test is translated to device temperatures using the Arrhenius relationship; exp (-Ea/kT), where Ea is the activation energy, k is the Boltzmann's constant, and T is the absolute temperature for the failure calculation. The important step in predicting the failure rate is to determine the failure mechanism and the corresponding failure activation energy. Ultimately this test is used to predict and model product reliability under user (field) conditions.

High Temperature Storage/Data Retention (Unbiased, 250°C)
The High Temperature Storage Test is used to thermally accelerate charge loss. This test verifies data retention, which is the ability of the memory device to retain a stored pattern in its cells over a prolonged period of time, with no external bias.

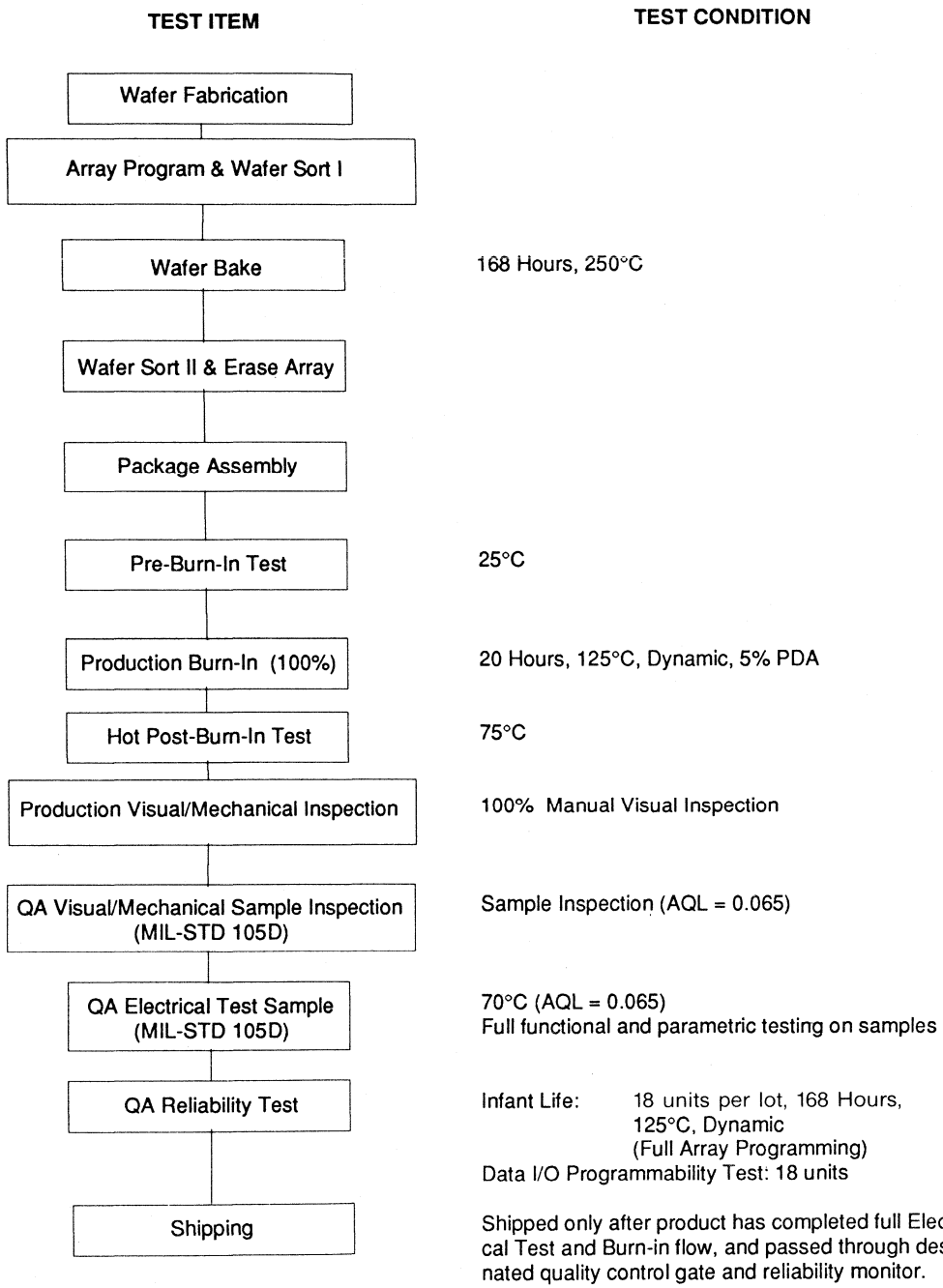
Temperature Humidity Bias (5.0V, 85°C, 85% R.H., Static)
Temperature Humidity Bias is used to accelerate failure mechanisms by applying static bias on alternate pins at a high temperature and humidity ambient (85°C/85% R.H.). This test checks for resistance to moisture penetration by using an electrolytic principle to accelerate corrosive mechanisms. Static bias is used to lessen the effects of thermal dissipation.

Pressure Cooker Test (Unbiased, 121°C, 15 PSIG, 100% R.H.)
The Pressure Cooker Test checks for resistance to moisture penetration. A pressurized vessel is used to force water (thereby promoting corrosion) into packaged devices located within the vessel.

Temperature Cycling (Unbiased, -65°C to +150°C, air-to-air)
This stress uses a chamber with alternating temperatures of -65°C and +150°C (air ambient) to thermally cycle devices. No bias is applied. The cycling checks for mechanical integrity of the packaged device, in particular bond wires and die attach, along with metal/polysilicon microcracks.

Thermal Shock (Unbiased, -65°C to +150°C, liquid-to-liquid)
This stress uses a chamber with alternating temperatures of -65°C and +150°C (liquid ambient) to thermally cycle devices. No bias is applied. The cycling checks for mechanical integrity of the packaged device, in particular bond wires and die attach, along with metal/polysilicon microcracks.

CPL PRODUCT OUTGOING TEST FLOW



Product Guide	*1*
Technical Overview/Quality and Reliability	*2*
Product Specifications	*3*
CPL Programming Electrical Specifications	*4*
CPL Starter Kit/CPL Programmer and Software Guide	*5*
Definition of Terms	*6*
Package Drawings	*7*
Sales Offices	*8*

CPL20 SERIES
CPL24 SERIES
CPL16V8
CPL20V8
CPL22V10

Features/Benefits
General Description
Logic Symbols and Pin Configurations
Functional Description
Logic Diagrams
Absolute maximum Ratings
Recommended Operating Conditions
DC Electrical Characteristics
AC Electrical Characteristics
Switching Waveforms

CPL20
(CPL16L8, CPL16R4, CPL16R6 and CPL16R8)

CMOS Programmable Logic Array
20-Pin Series

FEATURES/BENEFITS

- High-speed CMOS equivalent to Bipolar PAL devices
- CMOS UV-erasable EPROM cell to allow reprogrammability
- Low power (35mA Max. I_{CC}) and standard (70mA Max. I_{CC}) versions
- Four speed grades (t_{PD} = 15ns Max, t_{PD} = 20ns Max, t_{PD}=25ns Max, and t_{PD} = 35ns Max)
- Available over both commercial and industrial temperature ranges
- >2000V ESD input and output protection
- 100% functional and AC tested
- 100% programming tested
- Programmable security bit to prevent pattern duplication
- Register Preload for register configuration
- Programmable three-state outputs

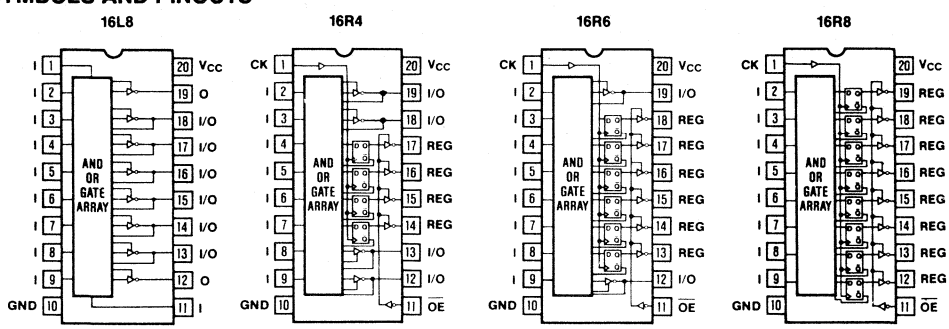
DESCRIPTION

The CPL20 Series devices are high-speed, UV-erasable, electrically programmable CMOS logic replacements of the Bipolar 20-pin PAL16R8 family. They utilize the familiar sum-of-products form (AND array followed by an OR array) allowing the user to customize logic to his/her needs.

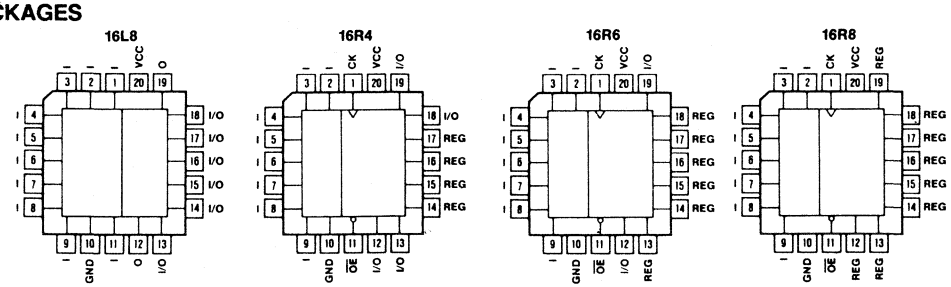
Four devices are offered in the CPL20 Series. They are: the CPL16L8, the CPL16R4, the CPL16R6, and the CPL16R8. Each of these devices has 16 array inputs and 8 outputs. All the outputs to the CPL16L8 are combinatorial, while all the outputs to the CPL16R8 are registered. In contrast, the CPL16R4 has 4 registered and 4 combinatorial outputs, and the CPL16R6 has 6 registered and 2 combinatorial outputs. Each combinatorial output in the CPL16R6 and CPL16R4 devices serves as an I/O pin. The CPL16L8 device has 6 I/O pins.

3

LOGIC SYMBOLS AND PINOUTS



DIP PACKAGES



PLCC PACKAGES

DESCRIPTION (Continued)

The CPL devices are manufactured using a 1.2 micron EPROM technology which offers low power dissipation (45/70 mA maximum I_{CC}) combined with high performance 15ns maximum propagation delay). Because the CPL devices are erasable, they can be thoroughly tested for programming, functional and AC integrity, resulting in high-reliability and 100% programming yields.

The CPL20 devices are housed in 20-pin plastic DIP, PLCC, and windowed CERDIP packages. The windowed CERDIP package allows the user to erase the CPL device using UV light, and later to reprogram it with a different pattern. The plastic DIP and PLCC devices are one-time-programmable (OTP) and may not be erased.

Register Preload

The register preload feature of the CPL20 Series allows output pins to be loaded with arbitrary states, making functional testing easier than ever.

Security Bit

All CPL20 devices feature a security bit. The security bit allows the user to protect his/her design against unauthorized duplication. When the security bit is set, the contents of the programmable-cell array may not be accessed in Read or Verify modes. Since the CPL devices do not have visible fuses, they offer enhanced security over what is available in bipolar PAL devices.

Test Array

Another feature of the devices in the CPL20 Series is the on-chip test array. It is programmed for final functional and AC testing of the devices after they have been packaged (even if the security bits have been programmed). In the normal operation of the device, the test arrays are not accessed. In the test mode of operation, only the input terms in the shaded portion of the functional block diagram are accessed. The test array facilitates high-reliability as well as simple and short testing.

ERASURE (windowed-CERDIP only)

The CPL devices will erase by light at wavelengths of under 4000 Angstroms. The window must be covered by an opaque label to prevent erasure by exposure to sunlight or fluorescent lighting.

Recommended dose of ultraviolet light for erasure:
Wavelength of 2537 Angstroms
(minimum dose -- 25 Wsec/cm^2)

If an ultraviolet lamp with a 12mW/cm^2 power rating is used, 30 to 35 minutes of erasure time will suffice. The lamp must be closer than 1 inch from the window to guarantee optimal erasing conditions. Exposure to high intensity UV light for an extended period of time may cause permanent damage to the CPL devices. The maximum dosage recommended is 7250 Wsec/cm^2.

CPL20 ABSOLUTE MAXIMUM RATINGS (Note 1)

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{CC}	-0.5 to +7.0	V
DC Input Voltage	V_{IN} ($\|I_{IN}\| \leqq 20mA$)	-3.0 to +7.0	V
Off-State DC Output Voltage	V_O	-0.5 to V_{CC} + 0.5	V
DC Programming Voltage		14.0	V
Storage Temperature	T_{STG}	-65 to +150	°C
Power Dissipation per Package	P_D (Note 2)	500	mW

Note 1: Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only, and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

Note 2: Power dissipation temperature derating:
Plastic Package (N): -12mW/°C from 65°C to 85°C
Ceramic Package (J): -12mW/°C from 100°C to 125°C

RECOMMENDED OPERATING CONDITIONS For CPL20-20, -25, and -35

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{CC}	4.5 to 5.5	V
DC Input and Output (Off-State) Voltages	V_{IN}, V_O (Note 3)	0 to V_{CC}	V
Operating Temperature Range, Commercial	T_A	0 to +70	°C
Operating Temperature Range, Industrial	T_A	-40 to +105	°C

3

RECOMMENDED OPERATING CONDITIONS For CPL20-15 (Preliminary)

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{CC}	4.75 to 5.25	V
DC Input and Output (Off-State) Voltages	V_{IN}, V_O (Note 3)	0 to V_{CC}	V
Operating Temperature Range, Commercial	T_A	0 to +70	°C
Operating Temperature Range, Industrial	T_A	-40 to +105	°C

Note 3: Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND).

CPL20 DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions

Parameter	Symbol	Test Conditions		Min	Max	Unit
Low Level Input Voltage	V_{IL}				0.8	V
High Level Input Voltage	V_{IH}			2.0		V
Input Current	I_{IN}	$0 < V_{IN} < V_{CC}$		-10	10	μA
Low Level Output Voltage	V_{OL}	V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24mA		0.5	V
High Level Output Voltage	V_{OH}	V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	I_{OH} = -3.2mA	2.4		V
Off-State Output Leakage Current	I_{OZL}	V_{CC} = Max, V_{IN} = V_{IH} or V_{IL}	V_O = 0.4V		-100	μA
	I_{OZH}		V_O = 2.4V		100	
Power Supply Current	I_{CC}	All inputs = GND V_{CC} = Max I_{OUT} = 0mA	"L" STD "L-15"		35 70 45	mA mA mA

Note 4: These are absolute values with respect to device ground. The applied voltage plus overshoots due to system and/or tester noise must not exceed these worst-case values.

CPL20 AC ELECTRICAL CHARACTERISTICS

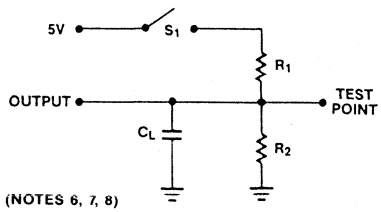
Over Recommended Operating Conditions (Note 5)

		Commercial (0 to +70°C)								Industrial (-40 to +105°C)								
		-15*		-20		-25		-35		-15*		-20		-25		-35		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Input or Feedback to Non-Registered Output, 16R6, 16R4, 16L8	t_{PD}		15		20		25		35		15		20		25		35	ns
Clock to Registered Output or Feedback, 16R8, 16R6, 16R4	t_{CO}		12		15		15		25		12		15		15		25	ns
Pin 11 to Output Enabled, 16R8, 16R6, 16R4	t_{PZX11}		12		15		20		25		12		15		20		25	ns
Pin 11 to Output Disabled, 16R8, 16R6, 16R4	t_{PXZ11}		12		15		20		25		12		15		20		25	ns
Input to Output Enabled, 16R6, 16R4, 16L8	t_{PZX}		15		20		25		35		15		20		25		35	ns
Input to Output Disabled, 16R6, 16R4, 16L8	t_{PXZ}		15		20		25		35		15		20		25		35	ns
Setup Time from Input or Feedback to Clock, 16R8, 16R6, 16R4	t_{SU}	12		15		20		30		12		15		20		30		ns
Hold Time, 16R8, 16R6, 16R4	t_H	0		0		0		0		0		0		0		0		ns
Clock Width (High or Low)	t_W	10		15		15		20		10		15		15		20		ns
Clock Period	t_P	24		30		35		55		24		30		35		55		ns
Maximum Frequency	f_{MAX}	41.6		33.3		28.5		18		41.6		33.3		28.5		18		MHz

* Preliminary

Note 5: Input rise and fall times (10% to 90% of V_{CC}): $t_r = t_f \leqq 6$ns.

AC Test Circuit



Resistor Values (Ω)

R1	R2
200	390

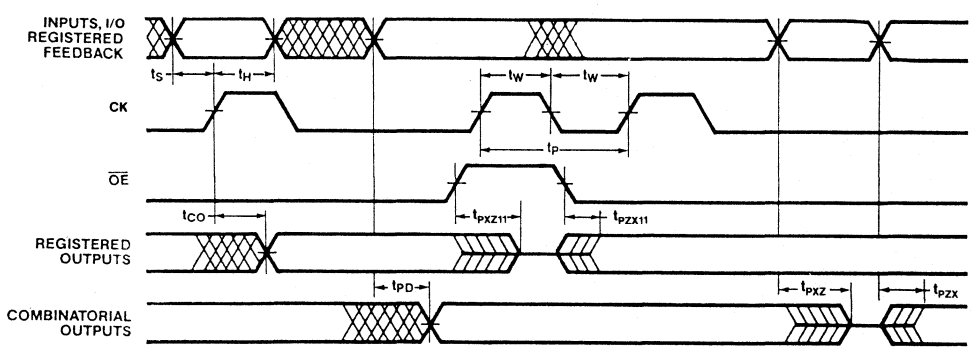
Note 6: C_L includes load and test jig capacitance.

Note 7: t_{PD} is tested with switch S_1 closed and C_L = 50pF.

Note 8: For 3-State outputs, output enable times are tested with C_L = 50pF to the 1.5V level; S_1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. Output disable times are tested with C_L = 5pF. HIGH to high impedance tests are made to an output voltage of V_{OH} - 0.5V with S_1 open; LOW to high impedance tests are made to the V_{OL} = 0.5V level with S_1 closed.

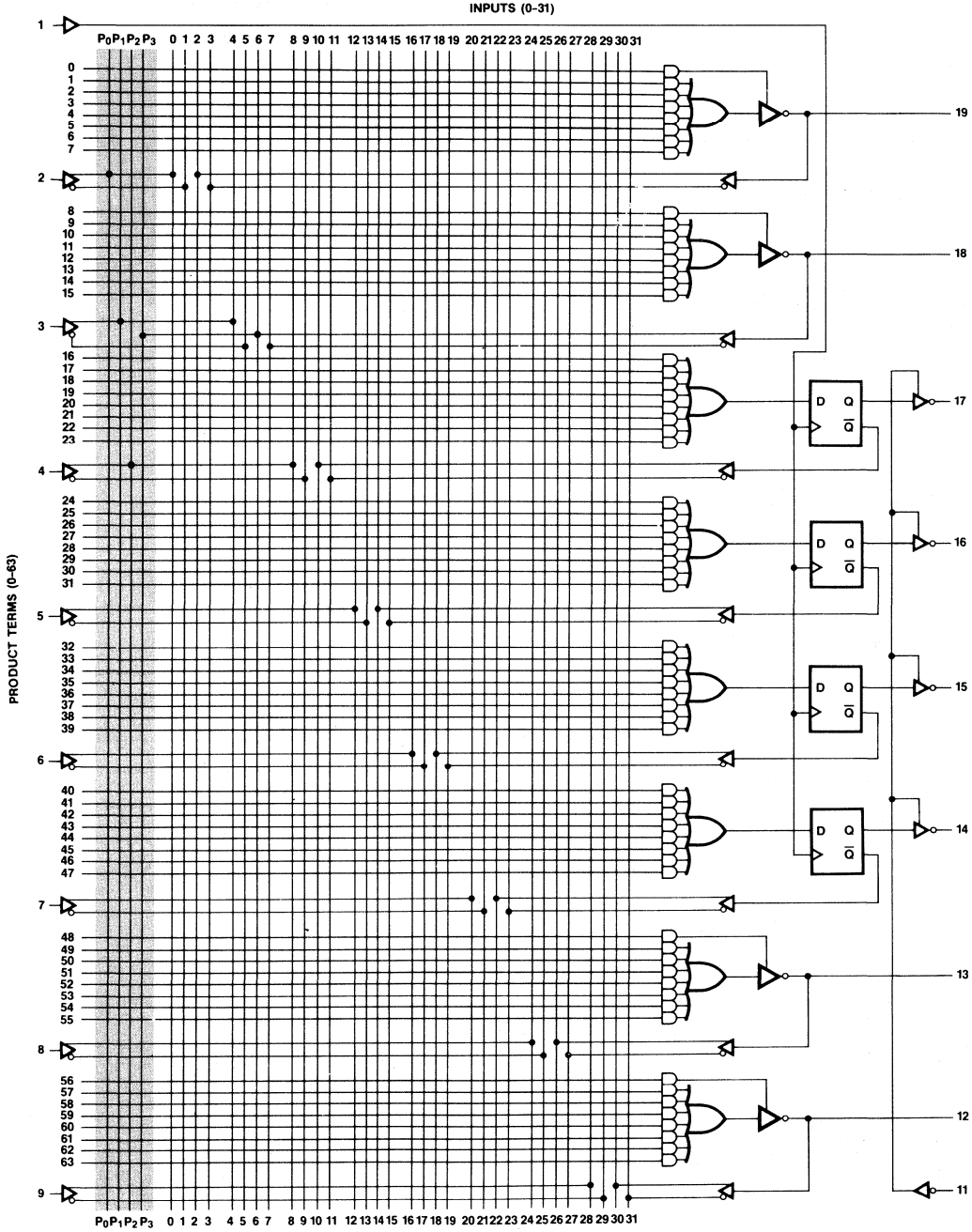
3

CPL20 SWITCHING WAVEFORMS



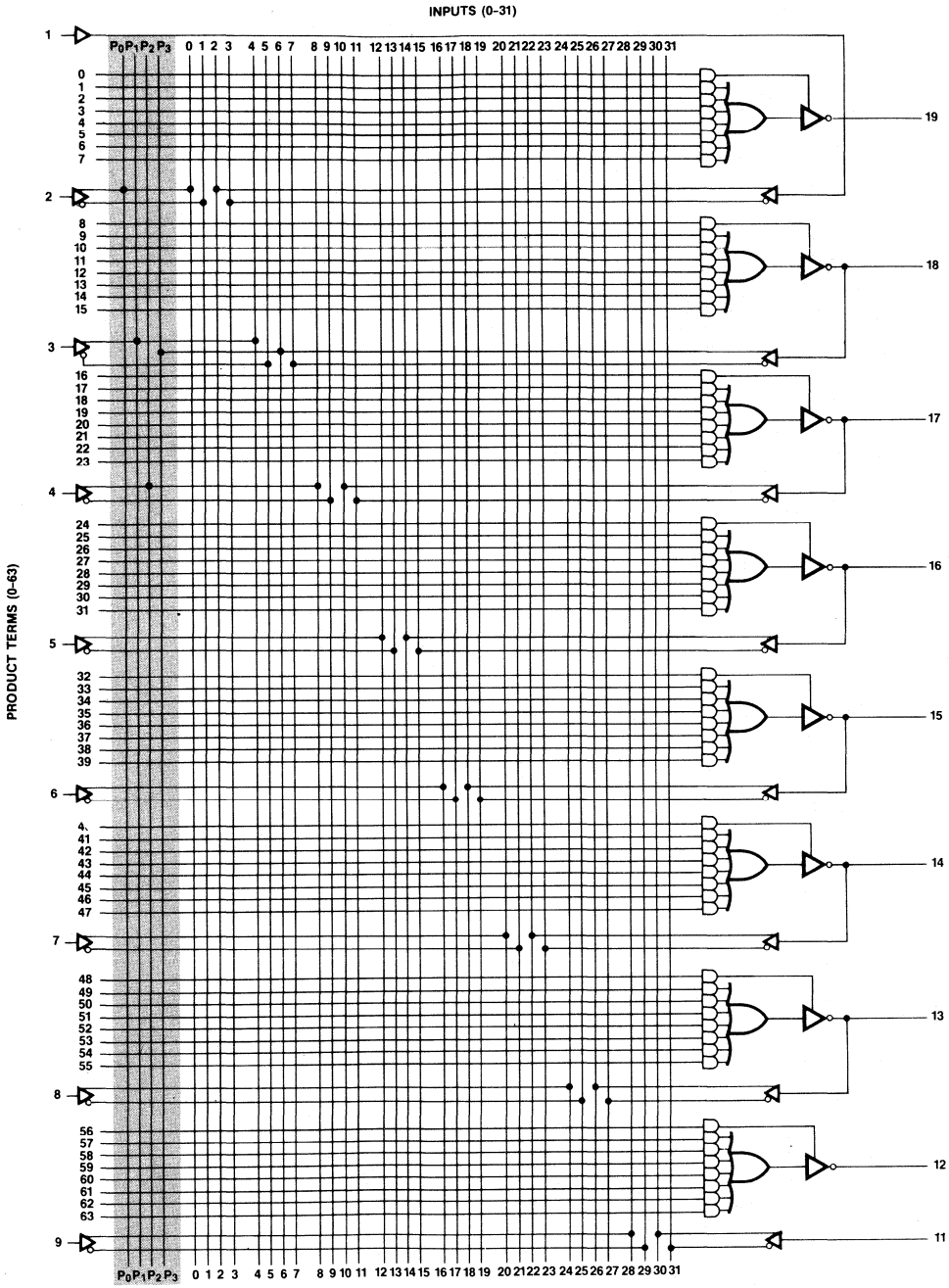
CPL20 FUNCTIONAL LOGIC DIAGRAMS (Continued)

CPL16R4



CPL20 FUNCTIONAL LOGIC DIAGRAMS

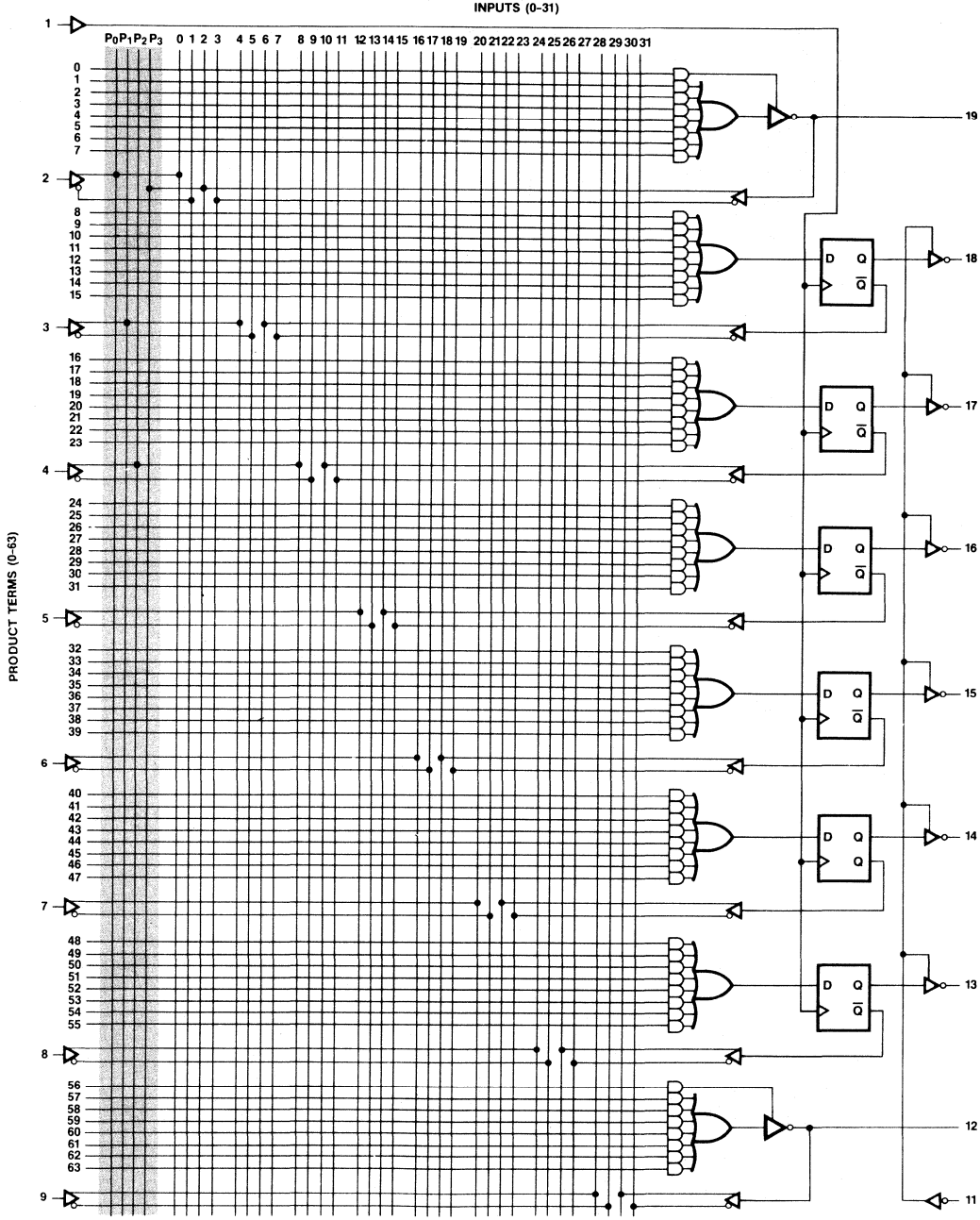
CPL16L8



3

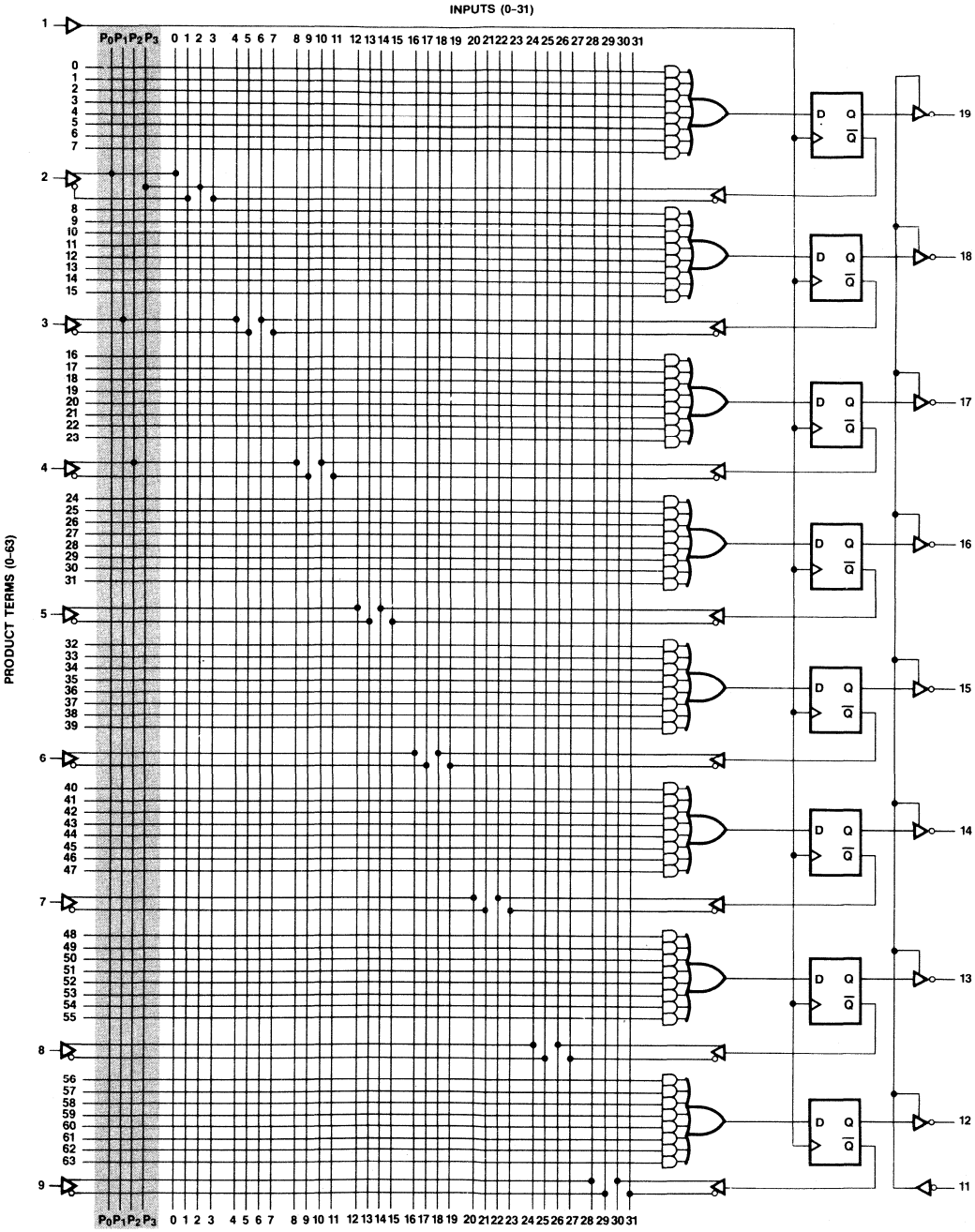
CPL20 FUNCTIONAL LOGIC DIAGRAMS (Continued)

CPL16R6



CPL20 FUNCTIONAL LOGIC DIAGRAMS (Continued)

CPL16R8



CPL24
(CPL20L8, CPL20R4, CPL20R6, CPL20R8 and CPL20L10)

CMOS Programmable Logic Array
24-Pin Series

FEATURES/BENEFITS

- High-speed CMOS equivalent to Bipolar PAL
- CMOS UV-erasable EPROM cell to allow reprogrammability
- Low power (35 mA Max. I_{CC}) and Standard (70 mA Max. I_{CC}) versions
- Four speed grades (t_{PD} = 15ns Max, t_{PD}=20ns Max, t_{PD}=25ns Max, and t_{PD} = 35ns Max)
- Available over both commercial and industrial temperature ranges
- >2000V ESD input and output protection
- 100% functional and AC tested
- 100% programming tested
- Programmable security bit to prevent pattern duplication
- Register preload for register initialization
- Programmable three-state outputs

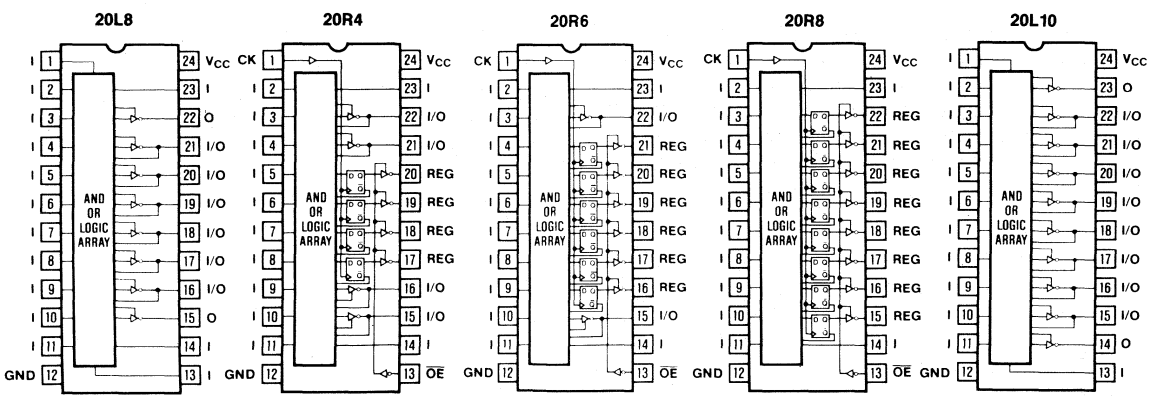
DESCRIPTION

The CPL24 Series devices are high-speed, UV-erasable, electrically programmable CMOS logic replacements of the Bipolar 24-pin PAL20R8 family and PAL20L10 devices. They utilize the familiar sum-of-products form (AND array followed by an OR array) allowing the user to customize logic to his/her needs.

Five devices are offered in the CPL24 Series. They are: the CPL20L10, the CPL20L8, the CPL20R4, the CPL20R6, and the CPL20R8. Each of these devices has 20 array inputs. The CPL20L10 has 10 outputs and the others have 8 outputs. All the outputs to the CPL20L8 and CPL20L10 are combinatorial, while all outputs to the CPL20R8 are registered. In contrast, the CPL20R4 has 4 registered and 4 combinatorial outputs and the CPL20R6 has 6 registered and 2 combinatorial outputs. Each combinatorial output in the CPL20R6 and CPL20R4 devices serves as an I/O pin. The CPL20L10 device has 8 I/O pins, and the CPL20L8 device has 6 I/O pins.

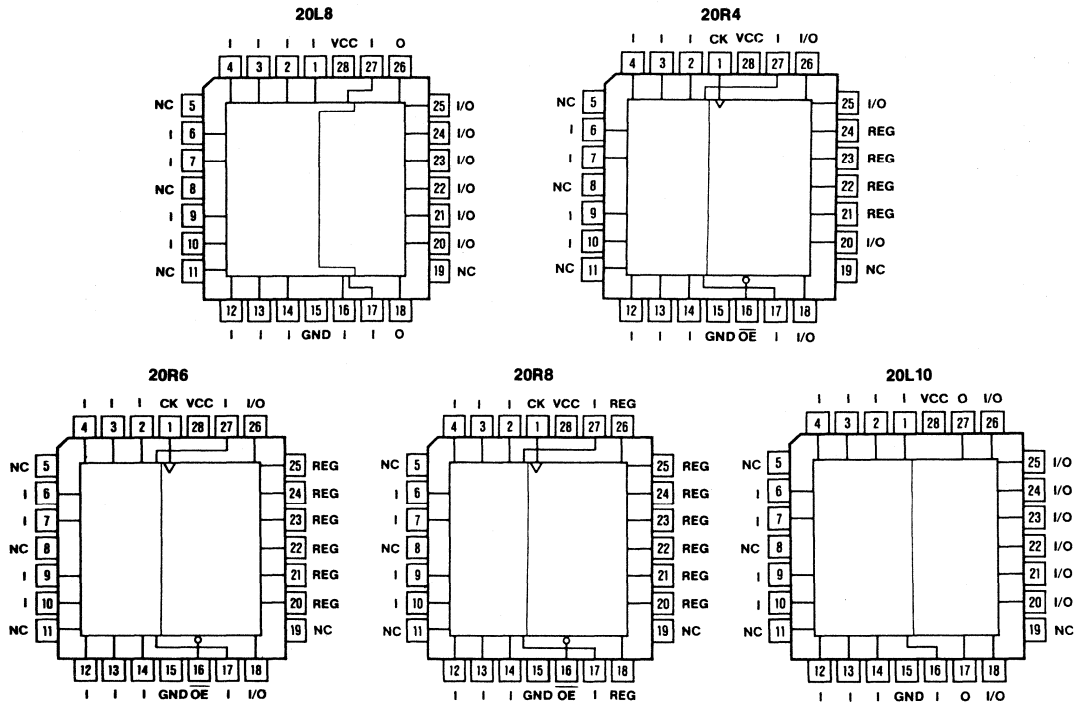
3

LOGIC SYMBOLS AND PINOUTS



DIP PACKAGES

LOGIC SYMBOLS AND PINOUTS (Continued)



PLCC PACKAGES (NL)

DESCRIPTION (Continued)

The CPL devices are manufactured using a 1.2 micron EPROM technology which offers low power dissipation (45/70 mA maximum I_{CC}) combined with high performance (15ns maximum propagation delay). Because the CPL devices are erasable, they can be thoroughly tested for programming, functional and AC integrity, resulting in high-reliability and 100% programming yields.

The CPL24 devices are housed in 24-pin plastic DIP, and windowed CERDIP packages, as well as a 28-pin PLCC package. The windowed CERDIP package allows the user to erase the CPL device using UV light, and later to reprogram it with a different pattern. The plastic DIP, and PLCC devices are one-time-programmable (OTP) and may not be erased.

Register Preload

The register preload feature of the CPL24 Series allows output pins to be loaded with arbitrary states, making functional testing easier than ever.

Security Bit

All CPL24 devices feature a security bit. The security bit allows the user to protect his/her design against unauthorized duplication. When the security bit is set, the contents of the programmable-cell array may not be accessed in Read or Verify modes. Since the CPL devices do not have visible fuses, they offer enhanced security over what is available in bipolar PAL devices.

Test Array

Another feature of the devices in the CPL24 Series is the on-chip test array. It is programmed for final functional and AC testing of the devices after they have been packaged (even if the security bits have been programmed). In the normal operation of the device, the test arrays are not accessed. In the test mode of operation, only the input terms in the shaded portion of the functional block diagram are accessed. The test array facilitates high-reliability as well as simple and short testing.

ERASURE (windowed-CERDIP only)

The CPL devices will erase by light at wavelengths of under 4000 Angstroms. The window must be covered by an opaque label to prevent erasure by exposure to sunlight or fluorescent lighting.

Recommended dose of ultraviolet light for erasure:

Wavelength of 2537 Angstroms
(minimum dose -- 25 Wsec/cm^2)

If an ultraviolet lamp with a 12mW/cm^2 power rating is used, 30 to 35 minutes of erasure time will suffice. The lamp must be closer than 1 inch from the window to guarantee optimal erasing conditions. Exposure to high intensity UV light for an extended period of time may cause permanent damage to the CPL devices. The maximum dosage recommended is 7250 Wsec/cm^2.

CPL24 ABSOLUTE MAXIMUM RATINGS (Note 1)

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{CC}	-0.5 to +7.0	V
DC Input Voltage	V_{IN} ($\|I_{IN}\| \leq$ 20mA)	-3.0 to +7.0	V
Off-State DC Output Voltage	V_O	-0.5 to V_{CC} + 0.5	V
DC Programming Voltage	V_{PP}	14.0	V
Storage Temperature	T_{STG}	-65 to +150	°C
Power Dissipation per Package	P_D (Note 2)	500	mW

Note 1: Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only, and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

Note 2: Power dissipation temperature derating:
Plastic Package (N): -12mW/°C from 65°C to 85°C
Ceramic Package (J): -12mW/°C from 100°C to 125°C

RECOMMENDED OPERATING CONDITIONS For all CPL24, except CPL24-15

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{CC}	4.5 to 5.5	V
DC Input and Output (Off-State) Voltages	V_{IN}, V_O (Note 3)	0 to V_{CC}	V
Operating Temperature Range, Commercial	T_A	0 to +70	°C
Operating Temperature Range, Industrial	T_A	-40 to +105	°C

RECOMMENDED OPERATING CONDITIONS For CPL24-15

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{CC}	4.75 to 5.25	V
DC Input and Output (Off-State) Voltages	V_{IN}, V_O (Note 3)	0 to V_{CC}	V
Operating Temperature Range, Commercial	T_A	0 to +70	°C
Operating Temperature Range, Industrial	T_A	-40 to +105	°C

Note 3: Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND).

DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions

Parameter	Symbol	Test Conditions		Min	Max	Unit
Low Level Input Voltage	V_{IL}				0.8	V
High Level Input Voltage	V_{IH}			2.0		V
Input Current	I_{IN}	$0 < V_{IN} < V_{CC}$		-10	10	μA
Low Level Output Voltage	V_{OL}	V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24mA		0.5	V
High Level Output Voltage	V_{OH}	V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	I_{OH} = -3.2mA	2.4		V
Off-State Output Leakage Current	I_{OZL}	V_{CC} = Max, V_{IN} = V_{IH} or V_{IL}	V_O = 0.4V		-100	μA
	I_{OZH}		V_O = 2.4V		100	
Power Supply Current	I_{CC}	All inputs = GND V_{CC} = Max I_{OUT} = 0mA	"L" STD "L-15"		35 70 45	mA mA mA

Note 4: These are absolute values with respect to device ground. The applied voltage plus overshoots due to system and/or tester noise must not exceed these worst-case values.

CPL24 AC ELECTRICAL CHARACTERISTICS, CPL20L10 only

Over Recommended Operating Conditions (Note 5)

		Commercial (0 to +70°C)								Industrial (-40 to +105°C)								
		-15		-20		-25		-30		-15*		-20		-25		-30		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Input or Feedback to Non-Registered Output, 20L10	t_{PD}		15		20		25		30		15		20		25		30	ns
Input to Output Enabled, 20L10	t_{PZX}		15		20		25		30		15		20		25		30	ns
Input to Output Disabled, 20L10	t_{PXZ}		15		20		25		30		15		20		25		30	ns
Clock Width (High or Low)	t_W	10		15		15		18		10		15		15		18		ns
Clock Period	t_P	24		30		35		40		24		30		35		40		ns
Maximum Frequency	f_{MAX}	41.6		33.3		28.5		25		41.6		33.3		28.5		25		MHz

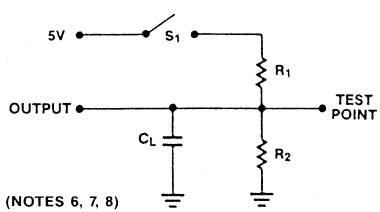
CPL24 AC ELECTRICAL CHARACTERISTICS, except CPL20L10

Over Recommended Operating Conditions (Note 5)

		Commercial (0 to +70°C)								Industrial (-40 to +105°C)								
		-15		-20		-25		-35		-15		-20		-25		-35		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Input or Feedback to Non-Registered Output, 20R6, 20R4, 20L8	t_{PD}		15		20		25		35		15		20		25		35	ns
Clock to Registered Output or Feedback, 20R8, 20R6, 20R4	t_{CO}		12		15		15		25		12		15		15		25	ns
Pin 13 to Output Enabled, 20R8, 20R6, 20R4	t_{PZX13}		12		15		20		25		12		15		20		25	ns
Pin 13 to Output Disabled, 20R8, 20R6, 20R4	t_{PXZ13}		12		15		20		25		12		15		20		25	ns
Input to Output Enabled, 20R6, 20R4, 20L8	t_{PZX}		15		20		25		35		15		20		25		35	ns
Input to Output Disabled, 20R6, 20R4, 20L8	t_{PXZ}		15		20		25		35		15		20		25		35	ns
Setup Time from Input or Feedback to Clock, 20R8, 20R6, 20R4	t_{SU}	12		15		20		30		12		20		20		30		ns
Hold Time, 20R8, 20R6, 20R4	t_H	0		0		0		0		0		0		0		0		ns
Clock Width (High or Low)	t_W	10		15		15		20		10		15		15		20		ns
Clock Period	t_P	24		30		35		55		24		30		35		55		ns
Maximum Frequency	f_{MAX}	41.6		33.3		28.5		18		41.6		33.3		28.5		18		MHz

Note 5: Input rise and fall times (10% to 90% of V_{CC}): $t_r = t_f \leqq 6$ns.

AC Test Circuit



Resistor Values (Ω)

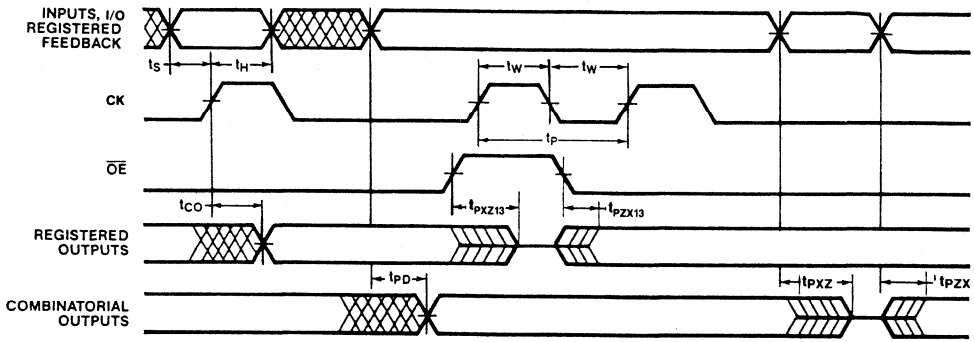
R1	R2
200	390

Note 6: C_L includes load and test jig capacitance.

Note 7: t_{PD} is tested with switch S_1 closed and C_L = 50pF.

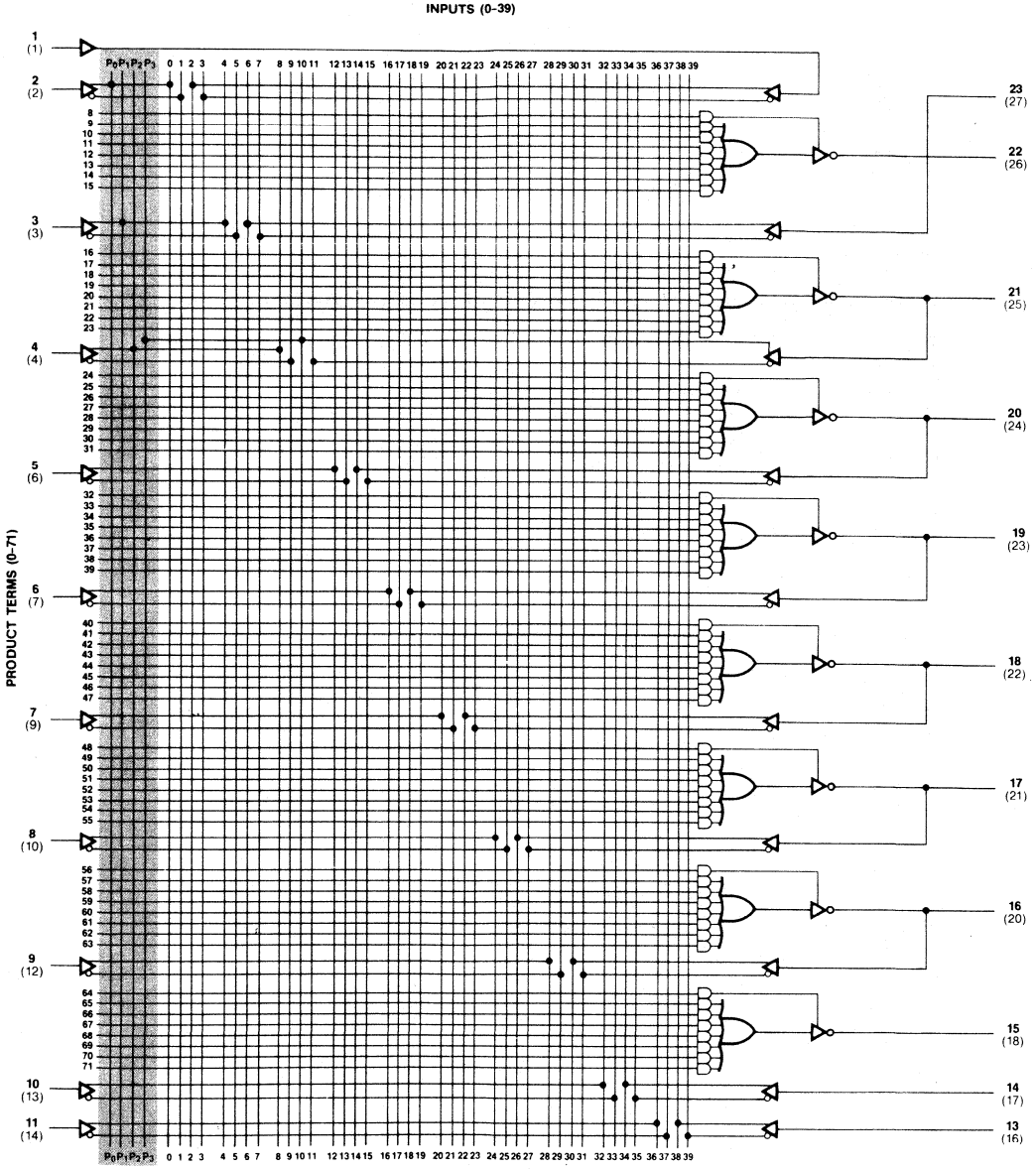
Note 8: For 3-State outputs, output enable times are tested with C_L = 50pF to the 1.5V level; S_1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. Output disable times are tested with C_L = 5pF. HIGH to high impedance tests are made to an output voltage of V_{OH} - 0.5V with S_1 open; LOW to high impedance tests are made to the V_{OL} = 0.5V level with S_1 closed.

CPL24 WAVEFORMS

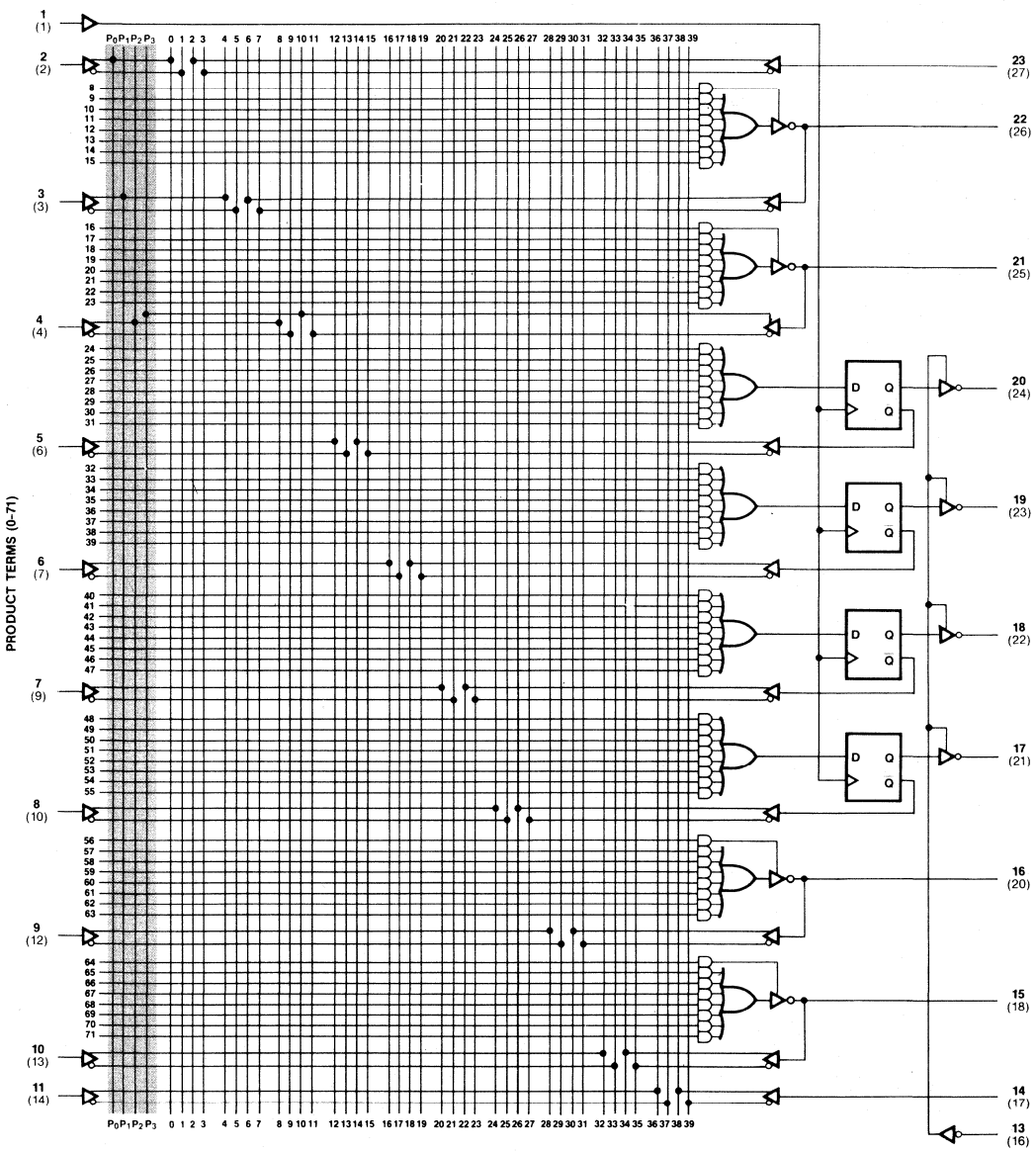


CPL24 FUNCTIONAL LOGIC DIAGRAMS (Continued)
DIP AND PLCC PINOUTS

CPL20L8

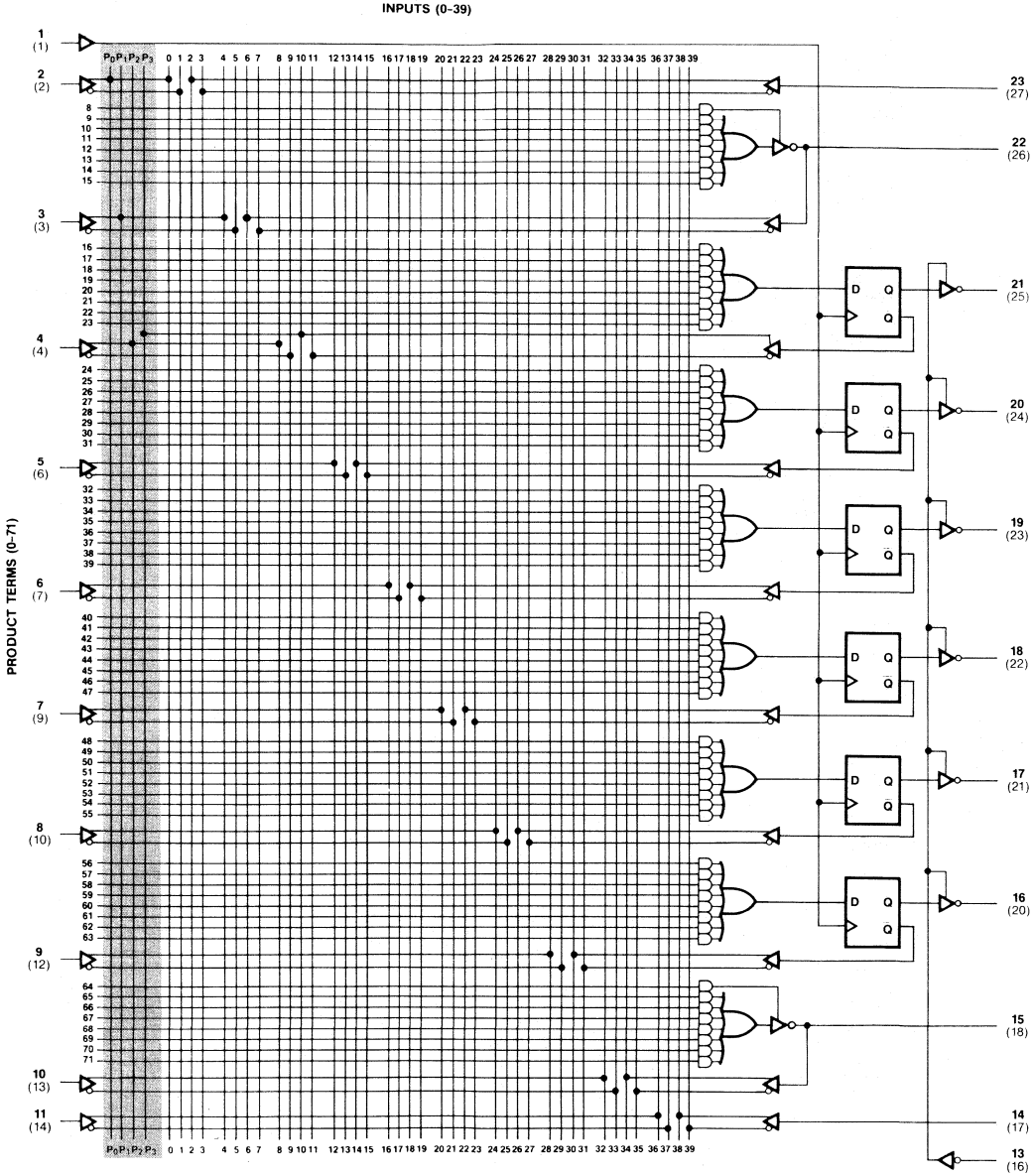


CPL20R4


INPUTS (0-39)
PRODUCT TERMS (0-71)
P0 P1 P2 P3 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39
1 (1)
2 (2)
3 (3)
4 (4)
5 (6)
6 (7)
7 (9)
8 (10)
9 (12)
10 (13)
11 (14)
23 (27)
22 (26)
21 (25)
20 (24)
19 (23)
18 (22)
17 (21)
16 (20)
15 (18)
14 (17)
13 (16)
D Q
Q

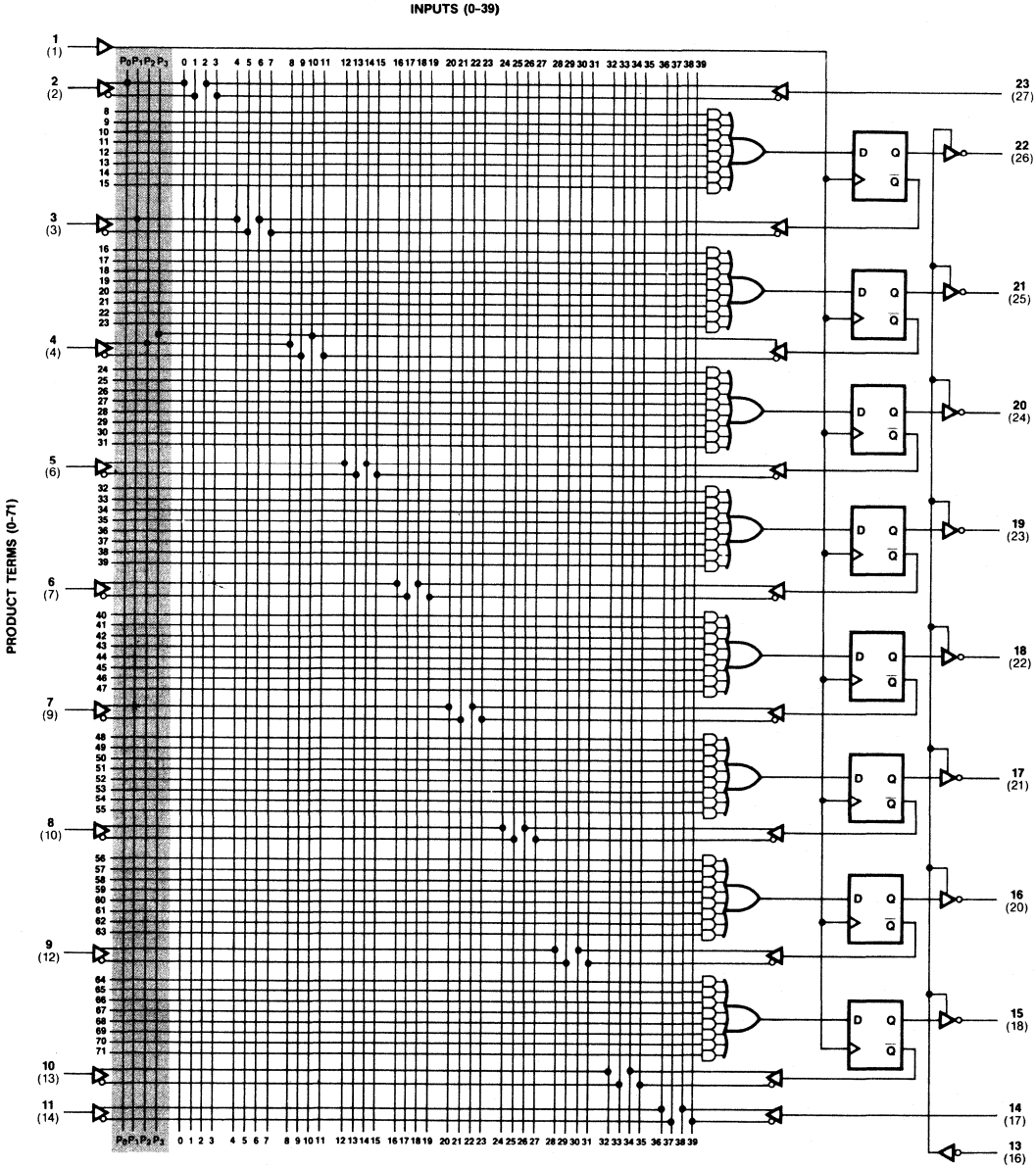
CPL24 FUNCTIONAL LOGIC DIAGRAMS (Continued)
DIP AND PLCC PINOUTS

CPL20R6

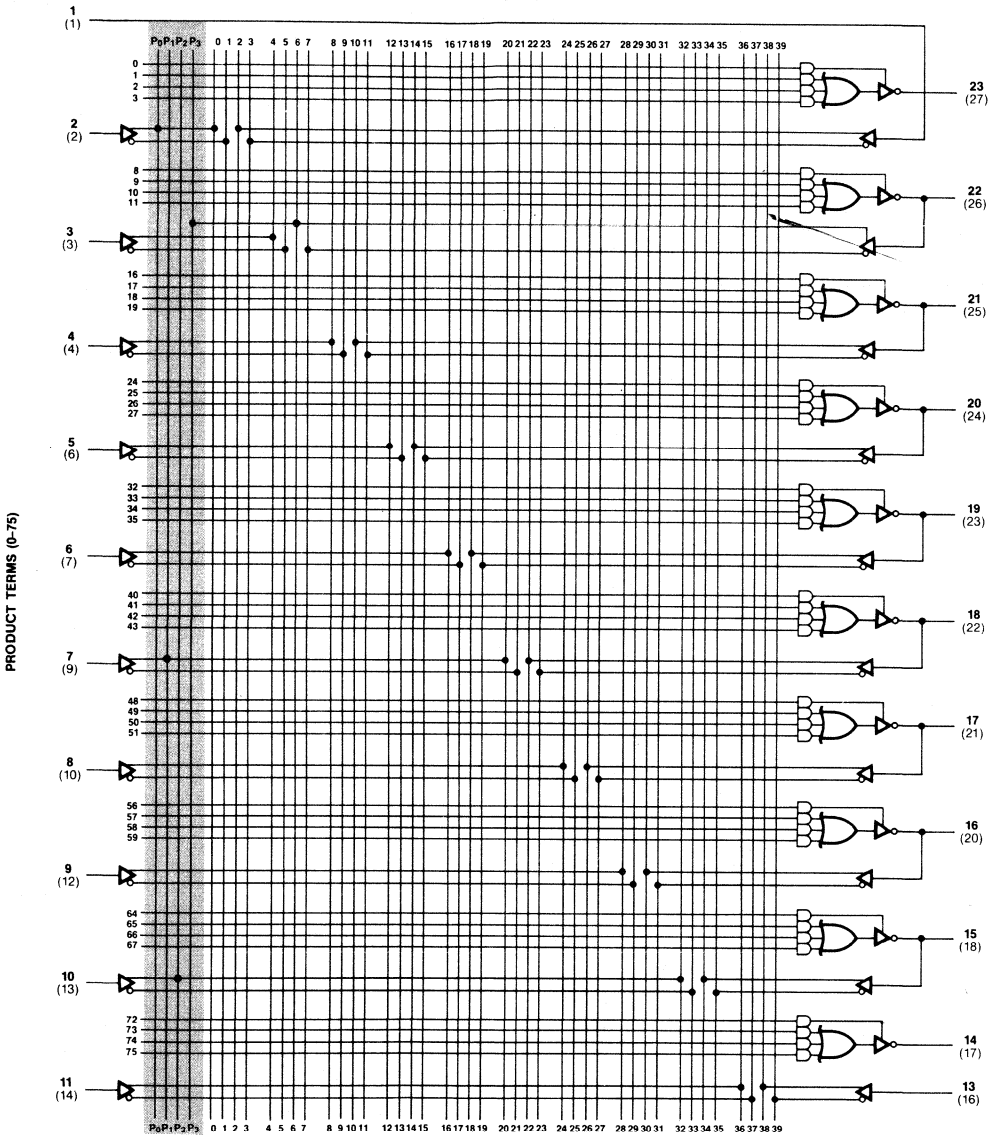


CPL24 FUNCTIONAL LOGIC DIAGRAMS (Continued)
DIP AND PLCC PINOUTS

CPL20R8



CPL20L10


INPUTS (0-39)
PRODUCT TERMS (0-75)
P0P1P2P3 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39
1 (1)
2 (2)
3 (3)
4 (4)
5 (6)
6 (7)
7 (9)
8 (10)
9 (12)
10 (13)
11 (14)
23 (27)
22 (26)
21 (25)
20 (24)
19 (23)
18 (22)
17 (21)
16 (20)
15 (18)
14 (17)
13 (16)

CPL16V8

CMOS PROGRAMMABLE LOGIC ARRAY WITH OUTPUT MACROCELLS (20-PIN)

Advance Information

FEATURES/BENEFITS

- **Equivalent to industry standard 16V8 architecture, superset of CPL20 family**
- **Three speed grades: t_{PD} = 20ns Max, t_{PD} = 25ns Max, t_{PD} = 30ns Max**
- **Two power grades: 45mA Max, 70mA Max**
- **CMOS, UV-erasable EPROM cell allows reprogrammability in windowed packages**
- **8 input/output macrocells for maximum flexibility**
  - **Up to 16 inputs and 8 outputs**
  - **Programmable output polarity**
  - **Registered or combinatorial output selection**
- **Test array and preloadable output registers for improved testability**
- **100% functional, AC and programming tests improve reliability and programming yields**
- **>2000V ESD input protection**
- **Programmable security bit to prevent CPL pattern duplication**

DESCRIPTION

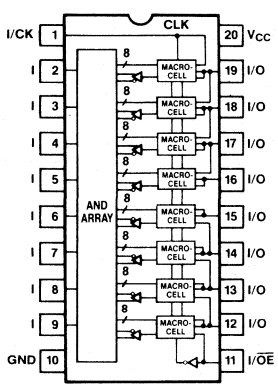
The CPL16V8 is a high-speed CMOS electrically programmable, UV-erasable device with an advanced architecture. The device is manufactured using a 1.2 micron EPROM technology offering low power dissipation combined with high performance. The UV-erasability of the device allows for 100% programming, functional, and AC testing, resulting in a highly reliable end product and 100% programming yields.

The CPL16V8 uses the standard programmable AND/Fixed OR logic array structure familiar to most programmable logic users to implement complex logic functions. The array is made up of 8 sets of product terms, each connected to a programmable macrocell via an OR gate. Eight product terms comprise each set, where they can be connected to 16 inputs, true or complement. Every output from the array feeds a programmable macrocell enabling it to be programmed as a combinatorial or registered, active high or low output.

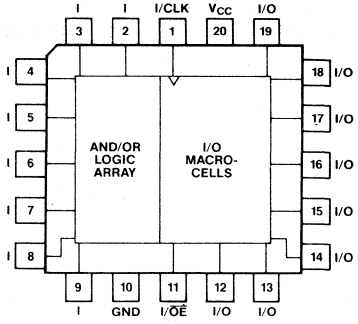
The 16V8 device can be housed in a 20-pin plastic DIP, 20-pin PLCC, or a windowed 20-pin CERDIP package. The windowed-CERDIP package allows the user to erase the CPL device using UV light, and later to reprogram it with a different pattern. The CPL device in a plastic package is One-Time-Programmable (OTP) and may not be erased.

3

PIN CONFIGURATIONS

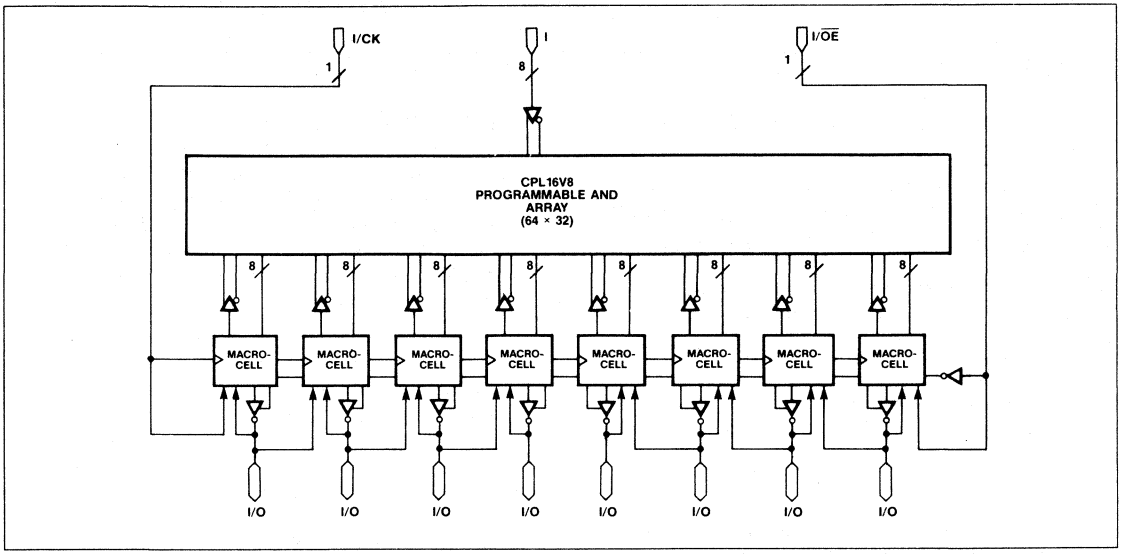


Dual In-Line Package



Plastic Leaded Chip Carrier

Figure 1. Block Diagram



The block diagram of the CPL16V8 device is shown in Figure 1. There are 10 dedicated inputs and 8 programmable macrocell outputs, which may also serve as inputs. In addition, pin 1 can act as a clock for the D-type registers and pin 11 can act as a common output enable. Each input and its complement is connected to a programmable AND array which contains a total of 64 product terms. Each set of 8 product terms drives an output macrocell.

CONFIGURABLE OUTPUT MACROCELLS

One of the CPL16V8's unique features is its 8 user-configurable output macrocells, shown in Figure 2a. By programming these macrocells, the device is not only capable of emulating all common 20-pin PAL device architectures, but also other architectures which have not previously been available.

There are three main PAL-like architectures that the CPL16V8 will emulate: programmed in Modes 0, 1, and 2:

Mode 0 — PAL architecture with Macrocells configured as Dedicated Inputs and/or Dedicated Combinatorial Outputs without Feedback.

Mode 1 — PAL architecture with all 8 Macrocells configured as Combinatorial Outputs, 6 with Feedback.

Mode 2 — PAL architecture with at least 1 Macrocell configured as a Registered Output. All Macrocells configured with Feedback.

These three modes are obtained by the programming of certain architectural control bits: SYN, AC0, AC1(n), and POL(n), which configure each macrocell in the CPL16V8. They are specified in the design file created during the design process and are completely transparent to the user.

A truth table in Figure 2b summarizes the output macrocell configurations that result when the architectural control bits are programmed.

REGISTERED OUTPUT CAPABILITY

Registered output capability is controlled by the SYN bit. If SYN is programmed HIGH (modes 0 and 1), the device outputs will be non-registered (asynchronous) and pins 1 and 11 stay as data inputs. If SYN is programmed LOW (mode 2), at least one output will be registered (synchronous) and pin 1 becomes the clock input while pin 11 becomes the common output enable for the registered output(s).

FUSE MAP COMPATIBILITY

The SYN bit is also used to maintain full JEDEC compatibility with standard 20-pin PAL device architectures. In mode 1, the SYN bit is inverted and replaces AC0 of the Input Feedback Multiplexer in the two outermost macrocells (pins 12, 19).

Figure 2a. Output Macrocell w/ Configuration Bits

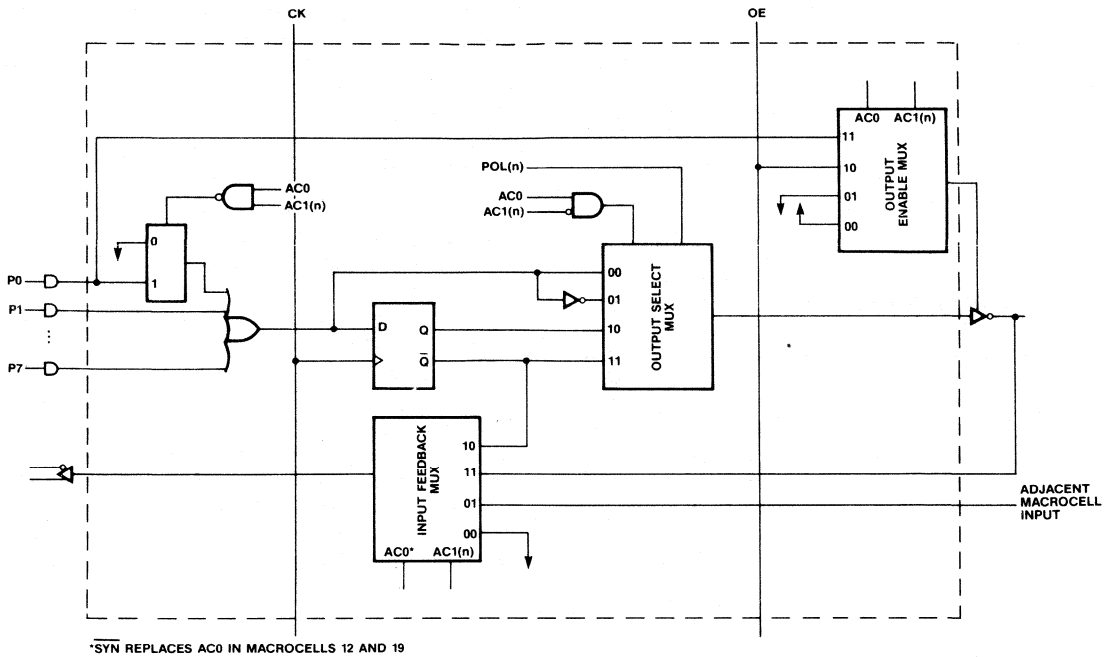


Figure 2b. Truth Table for Configuration Bits

Mode	SYN	AC0	AC1(n)	Output Macrocell Configuration	Notes
0	1	0	1	I/O Configured as Input, Output is Disabled.	Pins 1, 11 are data inputs. No feedback. Pins 15, 16 can only be outputs.
			0	I/O Configured as Dedicated Combinatorial Output, Output Always Enabled.	
1	1	1	1	All Outputs are Combinatorial — 16L8, 16H8, or 16P8 Configuration Only	Pins 1, 11 are data inputs. Pins 12, 19 can only be outputs.
2	0	1	1	I/O is Configured as Combinatorial Output in Registered Device	Pin 1 = $\overline{CK}$, Pin 11 = $\overline{OE}$
			0	I/O is Configured as Registered Output	

POL(n)	Output Polarity
0	Active Low
1	Active High

I/O AND OUTPUT ENABLE CONTROL

Input/Output control is selected via the AC0 control bit. If AC0 is programmed LOW (mode 0), each I/O is configured either as a dedicated input with the output always disabled, or as a dedicated combinatorial output with no feedback. If AC0 is programmed HIGH (modes 1 and 2), array feedback is allowed with the resultant outputs being combinatorial or registered.

Together with the AC0 bit, eight AC1(n) control bits individually determine the final configuration of each macrocell, except for the output's polarity. With AC0 LOW (mode 0), an AC1 bit programmed LOW will direct an I/O to be a dedicated input by disabling the macrocell's three-state output buffer, and an AC1 bit programmed HIGH will direct an I/O to be a dedicated output by permanently enabling the output buffer. With AC0 HIGH (modes 1 and 2), an AC1 bit programmed LOW will direct an output to be registered and have common output enable control, whereas an AC1 bit programmed HIGH will direct an output to be combinatorial and have the output enable controlled separately from a product term.

PROGRAMMABLE POLARITY

Finally, the polarity of each output macrocell is individually determined by the POL(n) bit. If POL(n) is programmed LOW, the macrocell output will be active LOW and if POL(n) is programmed HIGH, the output will be active HIGH.

EXAMPLE MACROCELL CONFIGURATIONS

Examples of the resultant CPL16V8 macrocell configurations for modes 0, 1, and 2 are illustrated in Figures 3, 4, and 5, respectively. Note that these three modes provide four main output configurations: combinatorial active low, combinatorial active high, registered active low, and registered active high.

When a registered output is chosen, the signal is shifted out on the positive clock transition to the I/O pin and also fed back into the array, providing current status information to the programmable array. This is important for state machine applications. When a combinatorial output is chosen or when the output is disabled and the signal is on the I/O pin, the signal is also fed back into the array, (except for pins 12 and 19 in mode 1).

Figure 3. Mode 0 Macrocell Configuration Example (Four I/O Cells)

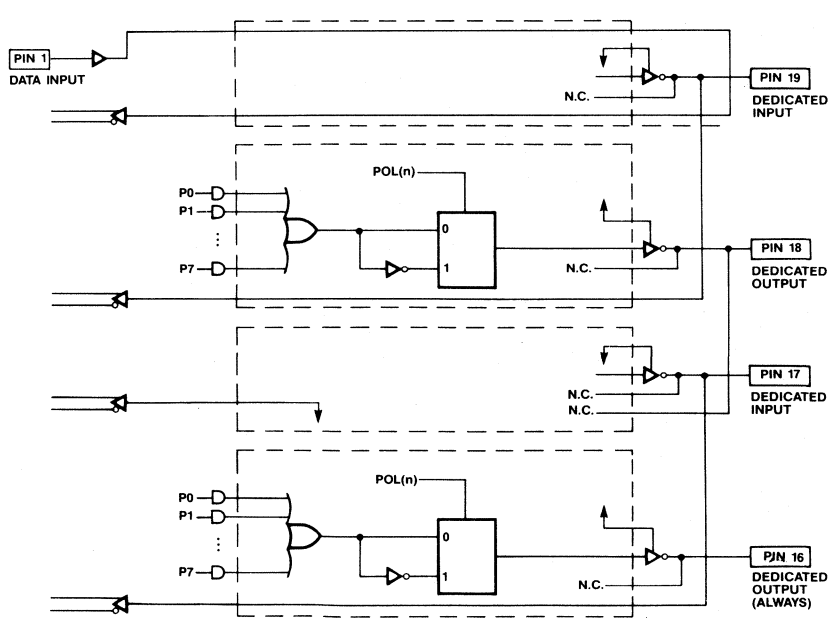


Figure 4. Mode 1 Macrocell Configuration Example (Two I/O Cells)

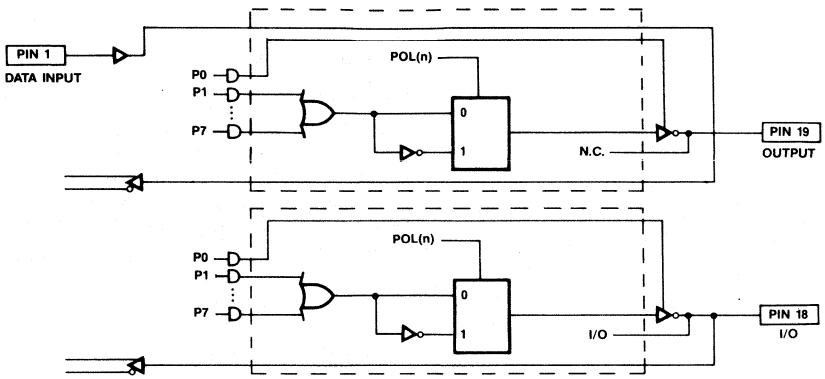
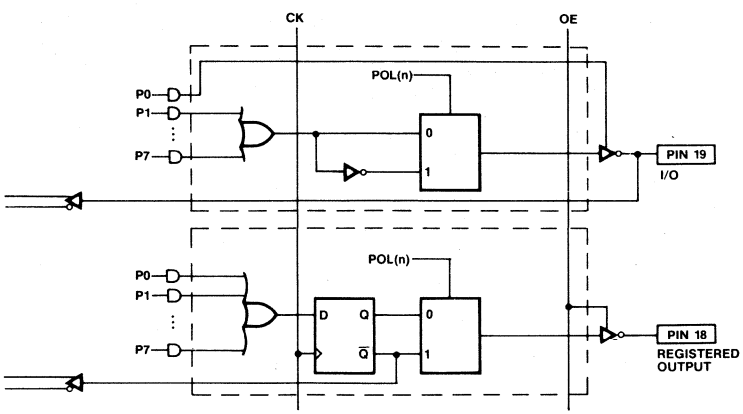


Figure 5. Mode 2 Macrocell Configuration Example (Two I/O Cells)



POWER-UP RESET

During system power-up, each register in the CPL16V8 will be reset to a logic low, to ensure predictable system initialization. Actual output states, however, will be low or high, depending on the polarity chosen at each output. For reliable resets, the V_{CC} rise must be monotonic and the clock input must not change for 1μs.

SECURITY BIT

To prevent a proprietary CPL16V8 design from being copied without authorization, a security bit has been provided. This security bit is programmed via the designer's logic programmer. Once this is done, the read, verify, and preload operations are disabled, which completely secures the device.

TEST FEATURES

Register Preload

To ease functional testing, the CPL16V8 device is equipped with a register preload feature that allows an arbitrary state value to be loaded into any or all of its registers from the output pins. This makes it possible to check and verify any logical state transition, without having to run through an entire test vector sequence. Also, by using register preload, all possible states can be tested to guarantee proper in-system operation.

Test Array

Another feature of the CPL16V8 is the on-chip test array which increases the device reliability by allowing each product term to be tested. The test array is programmed by Samsung to verify final functional and AC yields of the packaged device before shipping. When using the test array to test the device (even if the security bit has been programmed), only the input terms in the shaded portion of the functional block diagram are accessed. During normal operation, the test arrays are not accessed. As a result, the test array facilitates simple and shortened testing.

Input Term Testing

Finally, the CPL16V8 has additional product terms, one on output 12 and one on output 19, which are controlled by the device's input terms. These product terms allow testing of all input structures and are programmed for functional and AC testing of the packaged device, before shipping. The additional product terms are not accessed as part of the normal operation. Having both input term testing and test arrays allows Samsung to provide a packaged device of the highest quality.

ERASURE (windowed-CERDIP only)

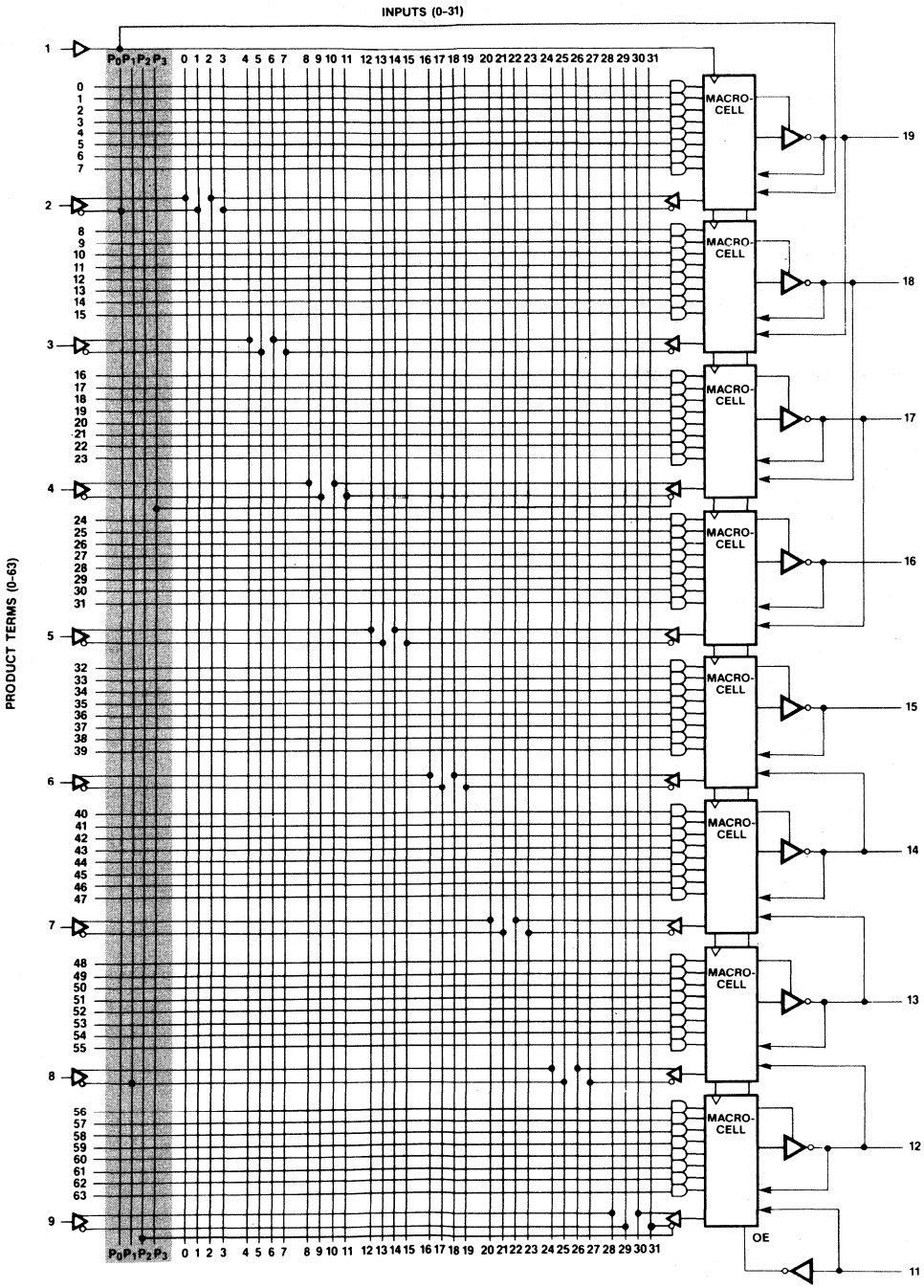
The CPL devices will erase by light at wavelengths of under 4000 Angstroms. The window must be covered by an opaque label to prevent erasure by exposure to sunlight or fluorescent lighting.

Recommended dose of ultraviolet light for erasure:

Wavelength of 2537 Angstroms
(minimum dose — 25 Wsec/cm^2)

If an ultraviolet lamp with a 12 mW/cm^2 power rating is used, 30 to 35 minutes of erasure time will suffice. The lamp must be closer than 1 inch from the window to guarantee optimal erasing conditions. Exposure to high intensity UV light for an extended period of time may cause permanent damage to the CPL devices. The maximum dosage recommended is 7250 Wsec/cm^2.

CPL16V8 FUNCTIONAL LOGIC DIAGRAM



CPL16V8 Absolute Maximum Ratings (Note 1)

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{CC}	-0.5 to +7.0	V
DC Input Voltage	V_{IN} ($\|I_{IN}\| \leq$ 20mA)	-3.0 to +7.0	V
Off-State DC Output Voltage	V_O	-0.5 to V_{CC} + 0.5	V
DC Programming Voltage	V_{PP}	14.0	V
Storage Temperature	T_{STG}	-65 to +150	°C
Power Dissipation per Package	P_D (Note 2)	500	mW

Note 1: Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only, and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.
Note 2: Power dissipation temperature derating:
Plastic Package (N): -12mW/°C from 65°C to 85°C
Ceramic Package (J): -12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{CC}	4.5 to 5.5	V
DC Input and Output (Off-State) Voltages	V_{IN}, V_O (Note 3)	0 to V_{CC}	V
Operating Temperature Range, Commercial	T_A	0 to +70	°C

Note 3: Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND).

DC Electrical Characteristics (Over Recommended Operating Conditions)

Parameter	Symbol	Test Conditions			Min	Max	Unit
Low Level Input Voltage	V_{IL}	(Note 4)				0.8	V
High Level Input Voltage	V_{IH}	(Note 4)			2.0		V
Input Current	I_{IN}	$0 < V_{IN} < V_{CC}$			-10	10	μA
Low Level Output Voltage	V_{OL}	V_{CC} = Min $V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 24mA			0.5	V
High Level Output Voltage	V_{OH}	V_{CC} = Min $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = -3.2mA		2.4		V
Off-State Output Leakage Current	I_{OZ}	V_{CC} = Max	$V_{SS} \leq V_O \leq V_{CC}$			±10	μA
Power Supply Current	I_{CC}	V_{IN} = GND, I_{OUT} = 0mA	V_{CC} = MAX	"L" STD		45 70	mA

Note 4: These are absolute values with respect to device ground. The applied voltage plus overshoots due to system and/or tester noise must not exceed these worst-case values.

Capacitance

Parameter	Description	Test Conditions	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1MHz		5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1MHz		8	

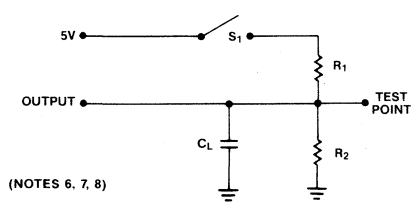
AC Electrical Characteristics

Over Recommended Operating Conditions (Note 5)

Parameter		Symbol	CPL16V8-20 COM/IND		CPL16V8-25 CPL16V8L-25 COM/IND		CPL16V8L-30 COM/IND		Unit
			Min	Max	Min	Max	Min	Max	
Input or Feedback to Non-Registered Output		t_{PD} (Note 8)		20		25		30	ns
Clock to Registered Output or Feedback		t_{CO}		15		15		20	ns
Pin 11 to Output Enabled		t_{PZX11}		18		20		25	ns
Pin 11 to Output Disabled		t_{PXZ11}		18		20		25	ns
Input to Output Enabled		t_{PZX}		20		25		30	ns
Input to Output Disabled		t_{PXZ}		20		25		30	ns
Setup Time from Input or Feedback to Clock		t_{SU}	15		20		25		ns
Hold Time		t_H	0		0		0		ns
Clock Width (High or Low)		t_W	12		15		15		ns
Clock Period		t_P	30		35		45		ns
Maximum Frequency	Feedback	f_{MAX}	33.3		28.5		22.2		MHz
	No Feedback		41.6		33.3		33.3		

Note 5: Input rise and fall times (10% to 90% of V_{CC}): $t_r = t_f \leqq 6ns$

AC Test Circuit



Resistor Values (Ω)

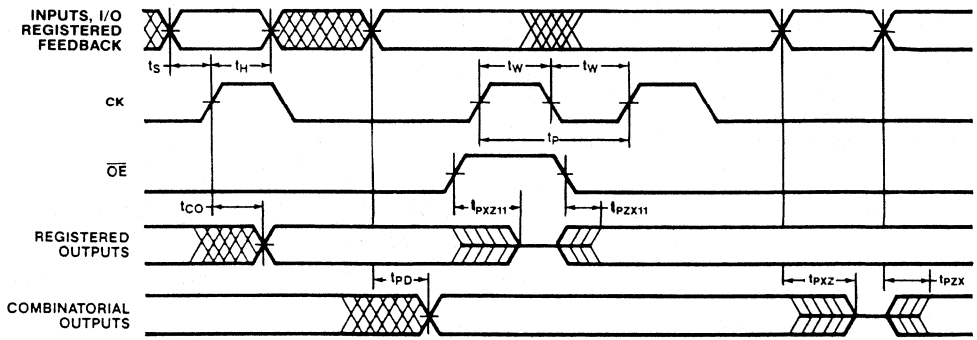
R1	R2
200	390

Note 6: C_L includes load and test jig capacitance.

Note 7: t_{PD} is tested with switch S_1 closed and C_L = 50pF.

Note 8: For 3-State outputs, output enable times are tested with C_L = 50pF to the 1.5V level; S_1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. Output disable times are tested with C_L = 5pF. HIGH to high impedance tests are made to an output voltage of V_{OH} - 0.5V with S_1 open; LOW to high impedance tests are made to the V_{OL} = 0.5V level with S_1 closed.

Switching Waveforms



CPL20V8

CMOS PROGRAMMABLE LOGIC ARRAY WITH OUTPUT MACROCELLS (24-PIN)

Advance Information

FEATURES/BENEFITS

- **Equivalent to industry standard 20V8 architecture, superset of CPL24 family**
- **Three speed grades:**
  t_{PD} = 20ns Max, t_{PD} = 25ns Max, t_{PD} = 30ns Max
- **Two power grades: 45mA Max, 70mA Max**
- **CMOS, UV-erasable EPROM cell allows reprogrammability in windowed packages**
- **8 input/output macrocells for maximum flexibility**
  - **— Up to 16 inputs and 8 outputs**
  - **— Programmable output polarity**
  - **— Registered or combinatorial output selection**
- **Test array and preloadable output registers for improved testability**
- **100% functional, AC and programming tests improve reliability and programming yields**
- **>2000V ESD input protection**
- **Programmable security bit to prevent CPL pattern duplication**

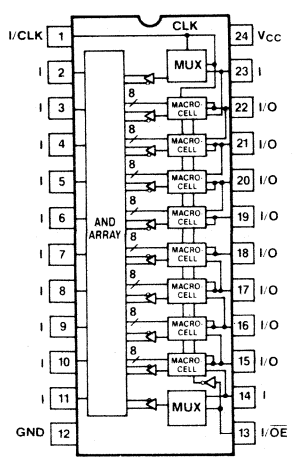
DESCRIPTION

The CPL20V8 is a high-speed CMOS electrically programmable, UV-erasable device with an advanced architecture. The device is manufactured using a 1.2 micron EPROM technology offering low power dissipation combined with high performance. The UV-erasability of the device allows for 100% programming, functional, and AC testing, resulting in a highly reliable end product and 100% programming yields.

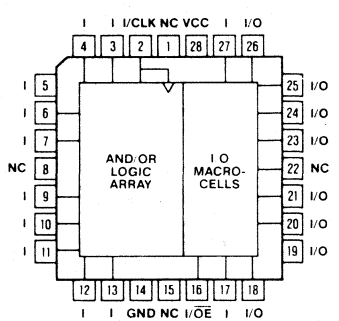
The CPL20V8 uses the standard programmable AND/Fixed OR logic array structure familiar to most programmable logic users to implement complex logic functions. The array is made up of 8 sets of product terms, each connected to a programmable macrocell via an OR gate. Eight product terms comprise each set, where they can be connected to 20 inputs, true or complement. Every output from the array feeds a programmable macrocell enabling it to be programmed as a combinatorial or registered, active high or low output.

The 20V8 device can be housed in a 24-pin plastic DIP, 28-pin PLCC, or a windowed 24-pin CERDIP package. The windowed-CERDIP package allows the user to erase the CPL device using UV light, and later to reprogram it with a different pattern. The CPL device in a plastic package is One-Time-Programmable (OTP) and may not be erased.

PIN CONFIGURATIONS

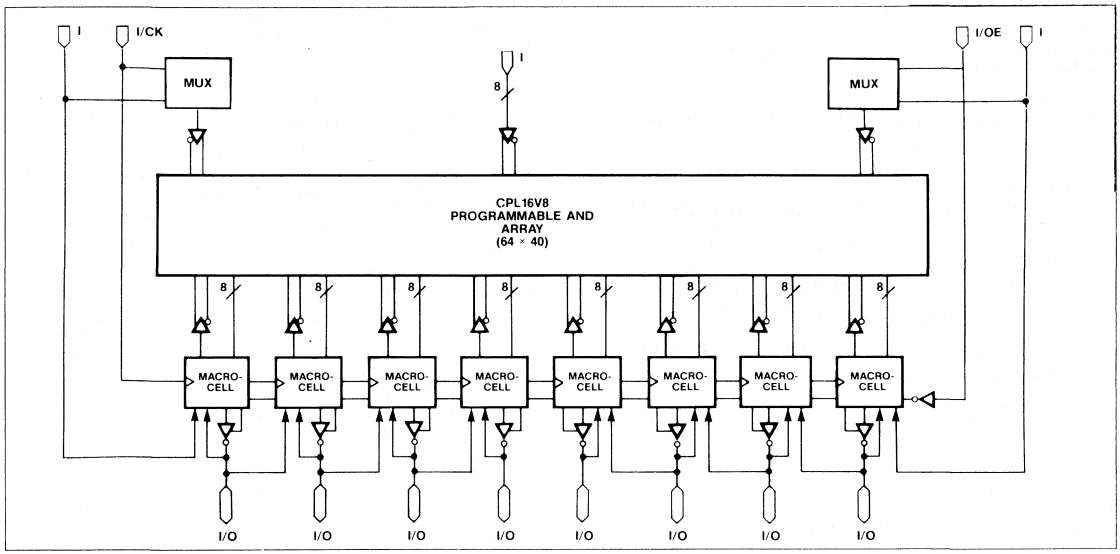


Dual In-Line Package



Plastic Leaded Chip Carrier

Figure 1. Block Diagram



The block diagram of the CPL20V8 device is shown in Figure 1. There are 14 dedicated inputs and 8 programmable macrocell outputs, which may also serve as inputs. In addition, pin 1 can act as a clock for the D-type registers and pin 13 can act as a common output enable. Each input and its complement is connected to a programmable AND array which contains a total of 64 product terms. Each set of 8 product terms drives an output macrocell.

CONFIGURABLE OUTPUT MACROCELLS

One of the CPL20V8's unique features is its 8 user-configurable output macrocells, shown in Figure 2a. By programming these macrocells, the device is not only capable of emulating all common 24-pin PAL device architectures, but also other architectures which have not previously been available.

There are three main PAL-like architectures that the CPL20V8 will emulate: programmed in Modes 0, 1, and 2:

Mode 0 — PAL architecture with Macrocells configured as Dedicated Inputs and/or Dedicated Combinatorial Outputs without Feedback.

Mode 1 — PAL architecture with all 8 Macrocells configured as Combinatorial Outputs, 6 with Feedback.

Mode 2 — PAL architecture with at least 1 Macrocell configured as a Registered Output. All Macrocells configured with Feedback.

These three modes are obtained by the programming of certain architectural control bits: SYN, AC0, AC1(n), and POL(n), which configure each macrocell in the CPL20V8. They are specified in the design file created during the design process and are completely transparent to the user.

A truth table in Figure 2b summarizes the output macrocell configurations that result when the architectural control bits are programmed.

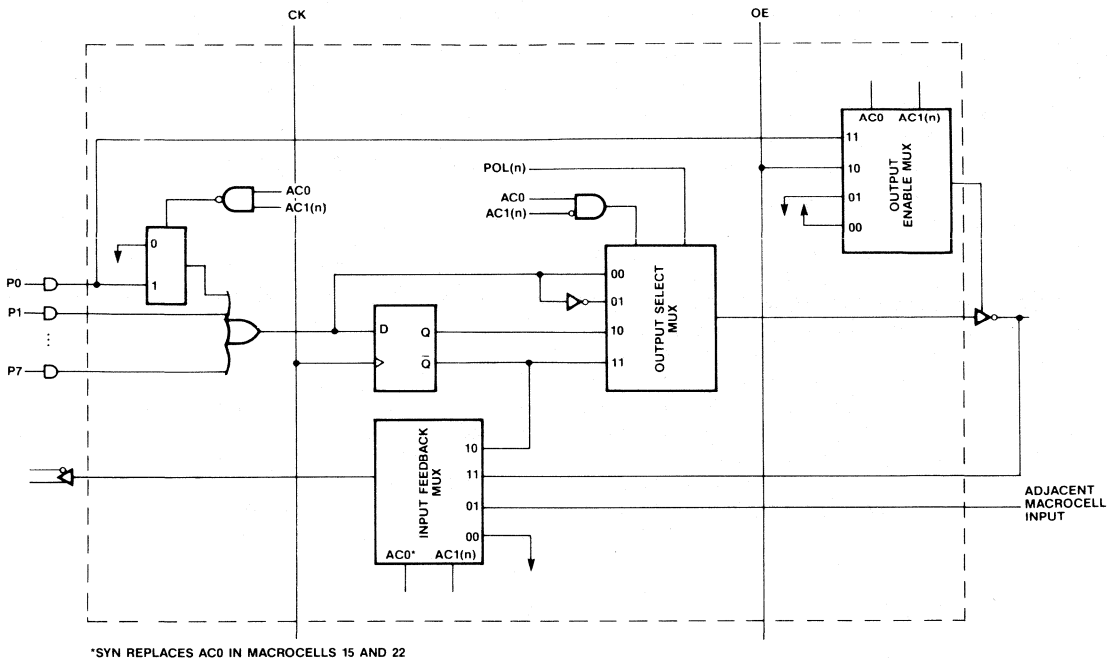
REGISTERED OUTPUT CAPABILITY

Registered output capability is controlled by the SYN bit. If SYN is programmed HIGH (modes 0 and 1), the device outputs will be non-registered (asynchronous) and pins 1 and 13 stay as data inputs. If SYN is programmed LOW (mode 2), at least one output will be registered (synchronous) and pin 1 becomes the clock input while pin 13 becomes the common output enable for the registered output(s).

FUSE MAP COMPATIBILITY

The SYN bit is also used to maintain full JEDEC fuse map compatibility with standard 24-pin PAL device architectures. In mode 1, the SYN bit is inverted and replaces AC0 of the Input Feedback Multiplexer of the outermost macrocells (pins 15, 22).

Figure 2a. Output Macrocell w/ Configuration Bits



*SYN REPLACES AC0 IN MACROCELLS 15 AND 22

Figure 2b. Truth Table for Configuration Bits

Mode	SYN	AC0	AC1(n)	Output Macrocell Configuration	Notes
0	1	0	1	I/O Configured as Input, Output is Disabled.	Pins 1, 13 are data inputs. No feedback. Pins 18, 19 can only be outputs.
			0	I/O Configured as Dedicated Combinatorial Output, Output Always Enabled.	
1	1	1	1	All Outputs are Combinatorial — 20L8, 20H8, or 20P8 Configuration Only	Pins 1, 13 are data inputs. Pins 15, 22 can only be outputs.
2	0	1	1	I/O is configured as Combinatorial Output in Registered Device	Pin 1 = CK, Pin 13 = $\overline{OE}$
			0	I/O is Configured as Registered Output	

POL(n)	Output Polarity
0	Active Low
1	Active High

I/O AND OUTPUT ENABLE CONTROL

Input/Output control is selected via the AC0 control bit. If AC0 is programmed LOW (mode 0), each I/O is configured either as a dedicated input with the output always disabled, or as a dedicated combinatorial output with no feedback. If AC0 is programmed HIGH (modes 1 and 2), array feedback is allowed with the resultant outputs being combinatorial or registered.

Together with the AC0 bit, eight AC1(n) control bits individually determine the final configuration of each macrocell, except for the output's polarity. With AC0 LOW (mode 0), an AC1 bit programmed LOW will direct an I/O to be a dedicated input by disabling the macrocell's three-state output buffer, and an AC1 bit programmed HIGH will direct an I/O to be a dedicated output by permanently enabling the output buffer. With AC0 HIGH (modes 1 and 2), an AC1 bit programmed LOW will direct an output to be registered and have common output enable control, whereas an AC1 bit programmed HIGH will direct an output to be combinatorial and have the output enable controlled separately from a product term.

PROGRAMMABLE POLARITY

Finally, the polarity of each output macrocell is individually determined by the POL(n) bit. If POL(n) is programmed LOW, the macrocell output will be active LOW and if POL(n) is programmed HIGH, the output will be active HIGH.

EXAMPLE MACROCELL CONFIGURATIONS

Examples of the resultant CPL20V8 macrocell configurations for modes 0, 1, and 2 are illustrated in Figures 3, 4, and 5, respectively. Note that these three modes provide four main output configurations: combinatorial active low, combinatorial active high, registered active low, and registered active high.

When a registered output is chosen, the signal is shifted out on the positive clock transition to the I/O pin and also fed back into the array, providing current status information to the programmable array. This is important for state machine applications. When a combinatorial output is chosen or when the output is disabled and the signal is on the I/O pin, the signal is also fed back into the array, (except for pins 15 and 22 in mode 1).

Figure 3. Mode 0 Macrocell Configuration Example (Four I/O Cells)

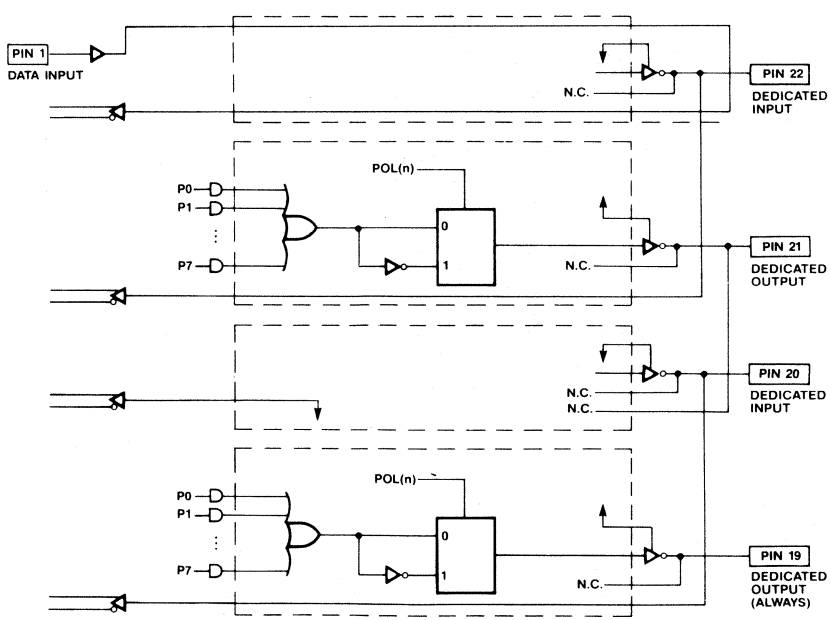


Figure 4. Mode 1 Macrocell Configuration Example (Two I/O Cells)

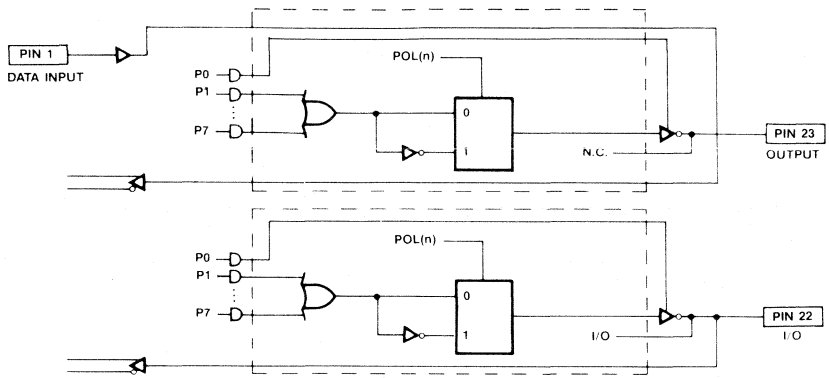
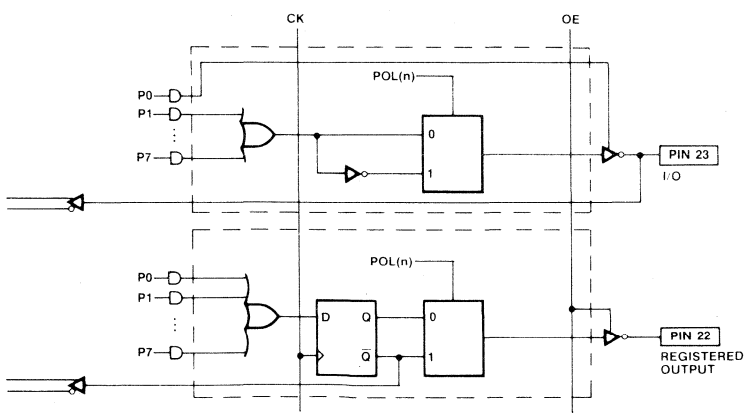


Figure 5. Mode 2 Macrocell Configuration Example (Two I/O Cells)



POWER-UP RESET

During system power-up, each register in the CPL20V8 will be reset to a logic low, to ensure predictable system initialization. Actual output states, however, will be low or high, depending on the polarity chosen at each output. For reliable resets, the V_{CC} rise must be monotonic and the clock input must not change for 1μs.

SECURITY BIT

To prevent a proprietary CPL20V8 design from being copied without authorization, a security bit has been provided. This security bit is programmed via the designer's logic programmer. Once this is done, the read verify, and preload operations are disabled, which completely secures the device.

TEST FEATURES

Register Preload

To ease functional testing, the CPL20V8 device is equipped with a register preload feature that allows an arbitrary state value to be loaded into any or all of its registers from the output pins. This makes it possible to check and verify any logical state transition, without having to run through an entire test vector sequence. Also, by using register preload, all possible states can be tested to guarantee proper in-system operation.

Test Array

Another feature of the CPL20V8 is the on-chip test array which increases the device reliability by allowing each product term to be tested. The test array is programmed by Samsung to verify final functional and AC yields of the packaged device before shipping. When using the test array to test the device (even if the security bit has been programmed), only the input terms in the shaded portion of the functional block diagram are accessed. During normal operation, the test arrays are not accessed. As a result, the test array facilitates simple and shortened testing.

Input Term Testing

Finally, the CPL20V8 has additional product terms, one on output 15 and one on output 22, which are controlled by the device's input terms. These product terms allow testing of all input structures and are programmed for functional and AC testing of the packaged device, before shipping. The additional product terms are not accessed as part of the normal operation. Having both input term testing and test arrays allows Samsung to provide a packaged device of the highest quality.

ERASURE (windowed-CERDIP only)

The CPL devices will erase by light at wavelengths of under 4000 Angstroms. The window must be covered by an opaque label to prevent erasure by exposure to sunlight or flourescent lighting.

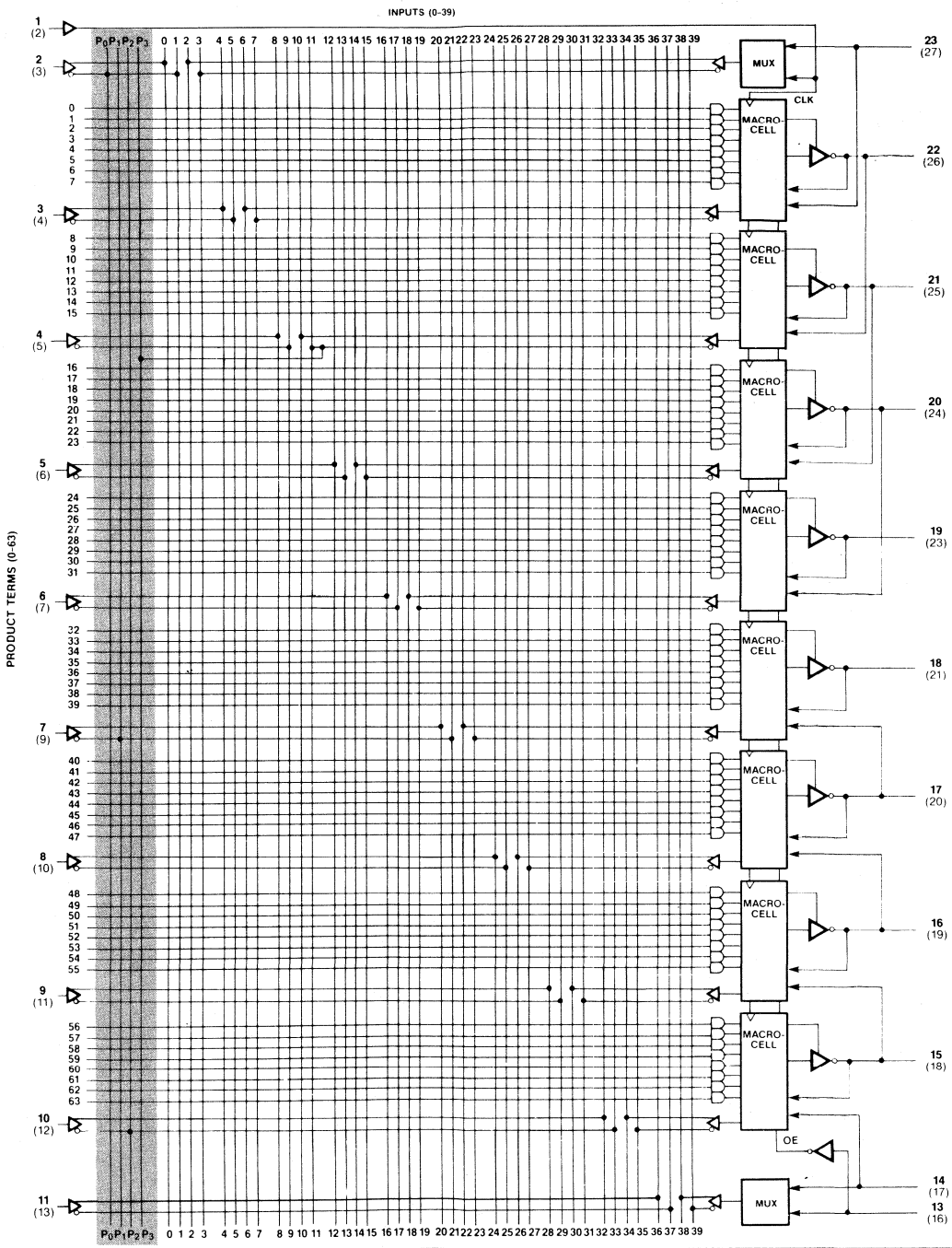
Recommended dose of ultraviolet light for erasure:

Wavelength of 2537 Angstroms
(minimum dose — 25 Wsec/cm^2)

If an ultraviolet lamp with a 12 mW/cm^2 power rating is used, 30 to 35 minutes of erasure time will suffice. The lamp must be closer than 1 inch from the window to guarantee optimal erasing conditions. Exposure to high intensity UV light for an extended period of time may cause permanent damage to the CPL devices. The maximum dosage recommended is 7250 Wsec/cm^2.

CPL20V8 FUNCTIONAL LOGIC DIAGRAM

DIP AND PLCC PINOUTS



CPL20V8 Absolute Maximum Ratings (Note 1)

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{CC}	-0.5 to +7.0	V
DC Input Voltage	V_{IN} ($\|I_{IN}\| \leq$ 20mA)	-3.0 to +7.0	V
Off-State DC Output Voltage	V_O	-0.5 to V_{CC} + 0.5	V
DC Programming Voltage	V_{PP}	14.0	V
Storage Temperature	T_{STG}	-65 to +150	°C
Power Dissipation per Package	P_D (Note 2)	500	mW

Note 1: Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only, and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

Note 2: Power dissipation temperature derating:
Plastic Package (N): -12mW/°C from 65°C to 85°C
Ceramic Package (J): -12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{CC}	4.5 to 5.5	V
DC Input and Output (Off-State) Voltages	V_{IN}, V_O (Note 3)	0 to V_{CC}	V
Operating Temperature Range, Commercial	T_A	0 to +70	°C

Note 3: Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND).

DC Electrical Characteristics (Over Recommended Operating Conditions)

Parameter	Symbol	Test Conditions			Min	Max	Unit
Low Level Input Voltage	V_{IL}	(Note 4)				0.8	V
High Level Input Voltage	V_{IH}	(Note 4)			2.0		V
Input Current	I_{IN}	$0 < V_{IN} < V_{CC}$			-10	10	μA
Low Level Output Voltage	V_{OL}	V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24mA			0.5	V
High Level Output Voltage	V_{OH}	V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	I_{OH} = -3.2mA		2.4		V
Off-State Output Leakage Current	I_{OZ}	V_{CC} = Max	$V_{SS} \leq V_O \leq V_{CC}$			±10	μA
Power Supply Current	I_{CC}	V_{IN} = GND, I_{OUT} = 0mA	V_{CC} = MAX	"L" STD		45 70	mA

Note 4: These are absolute values with respect to device ground. The applied voltage plus overshoots due to system and/or tester noise must not exceed these worst-case values.

Capacitance

Parameter	Description	Test Conditions	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1MHz		5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1MHz		8	

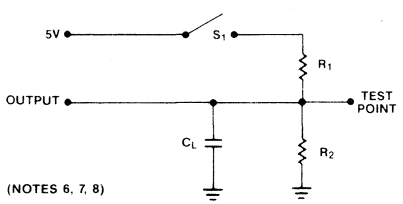
AC Electrical Characteristics

Over Recommended Operating Conditions (Note 5)

Parameter		Symbol	CPL20V8-20 COM/IND Min	CPL20V8-20 COM/IND Max	CPL20V8-25 CPL20V8L-25 COM/IND Min	CPL20V8-25 CPL20V8L-25 COM/IND Max	CPL20V8L-30 COM/IND Min	CPL20V8L-30 COM/IND Max	Unit
Input or Feedback to Non-Registered Output		t_{PD} (Note 8)		20		25		30	ns
Clock to Registered Output or Feedback		t_{CO}		15		15		20	ns
Pin 13 to Output Enabled		t_{PZX11}		18		20		25	ns
Pin 13 to Output Disabled		t_{PXZ11}		18		20		25	ns
Input to Output Enabled		t_{PZX}		20		25		30	ns
Input to Output Disabled		t_{PXZ}		20		25		30	ns
Setup Time from Input or Feedback to Clock		t_{SU}	15		20		25		ns
Hold Time		t_H	0		0		0		ns
Clock Width (High or Low)		t_W	12		15		15		ns
Clock Period		t_P	30		35		45		ns
Maximum Frequency	Feedback	f_{MAX}	33.3		28.5		22.2		MHz
	No Feedback		41.6		33.3		33.3		

Note 5: Input rise and fall times (10% to 90% of V_{CC}): $t_r = t_f \leqq 6ns$

AC Test Circuit



Resistor Values (Ω)

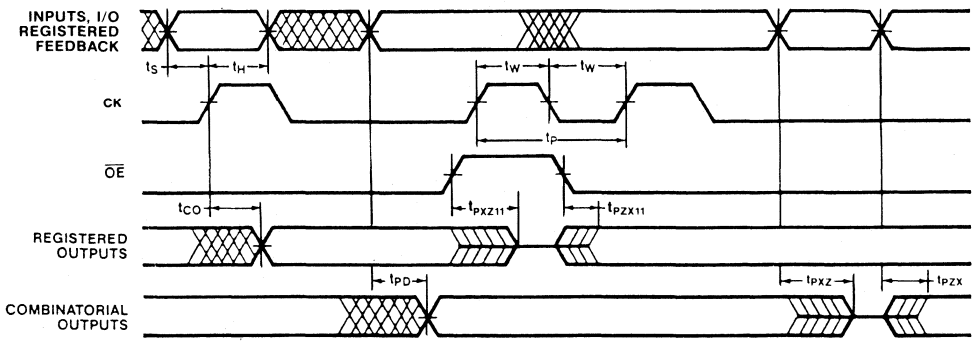
R1	R2
200	390

Note 6: C_L includes load and test jig capacitance.

Note 7: t_{PD} is tested with switch S_1 closed and C_L = 50pF.

Note 8: For 3-State outputs, output enable times are tested with C_L = 50pF to the 1.5V level; S_1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. Output disable times are tested with C_L = 5pF. HIGH to high impedance tests are made to an output voltage of V_{OH} - 0.5V with S_1 open; LOW to high impedance tests are made to the V_{OL} + 0.5V level with S_1 closed.

Switching Waveforms



CPL22V10

CMOS PROGRAMMABLE LOGIC ARRAY WITH OUTPUT MACROCELLS (24-PIN)

FEATURES/BENEFITS

- **Low power CMOS programmable alternative to bipolar 22V10 PLDs**
- **Two speed grades:**
  t_{PD} = 25ns Max, t_{PD} = 35ns Max
- **Two power grades: 55mA Max, 90mA Max**
- **CMOS, UV-erasable EPROM cell allows reprogrammability in windowed packages**
- **10 input/output macrocells for maximum flexibility**
  - **Up to 22 inputs and 10 outputs**
  - **Programmable output polarity**
  - **Registered or combinatorial output selection**
  - **Programmable feedback path**
- **Variable product term distribution**
  - **From 8 to 16 product terms available per output**
- **Global synchronous preset and asynchronous reset of all registers**
- **Registers reset on power-up**
- **Test arrays and preloadable output registers improve testability**
- **100% functional, AC, DC, and programming tests improve reliability and programming yields**
- **>2000V ESD input protection**
- **Security bit prevents CPL pattern duplication**

DESCRIPTION

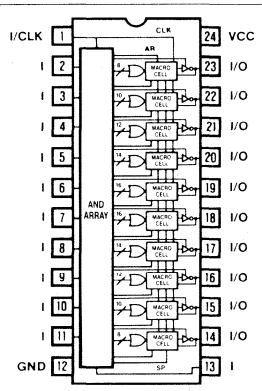
The CPL22V10 is a high-speed CMOS electrically programmable, UV-erasable device with an advanced architecture. The device is manufactured using Samsung's 1.2 micron EPROM technology offering low power dissipation combined with high performance. The UV-erasability of the device allows for 100% programming, functional, DC, and AC testing, resulting in a highly reliable end product and 100% programming yields.

The CPL22V10 uses the standard programmable AND/Fixed OR logic array structure familiar to most programmable logic users to implement complex logic functions. The array is made up of 10 sets of product terms, each connected to a programmable macrocell via an OR gate. Each set contains from 8 to 16 product terms where each product term can be connected to 22 inputs, true or complement. Each of the 10 OR array outputs feeds a programmable macrocell enabling it to be programmed as a combinatorial or registered, active high or low output.

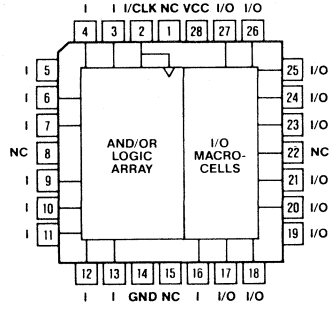
The CPL22V10 device can be housed in a 24-pin plastic DIP, 28-pin PLCC, or a windowed 24-pin CERDIP package. The windowed-CERDIP package allows the user to erase the CPL device using UV light, and later to reprogram it with a different pattern. The CPL device in a plastic package is One-Time-Programmable (OTP) and may not be erased.

3

PIN CONFIGURATIONS

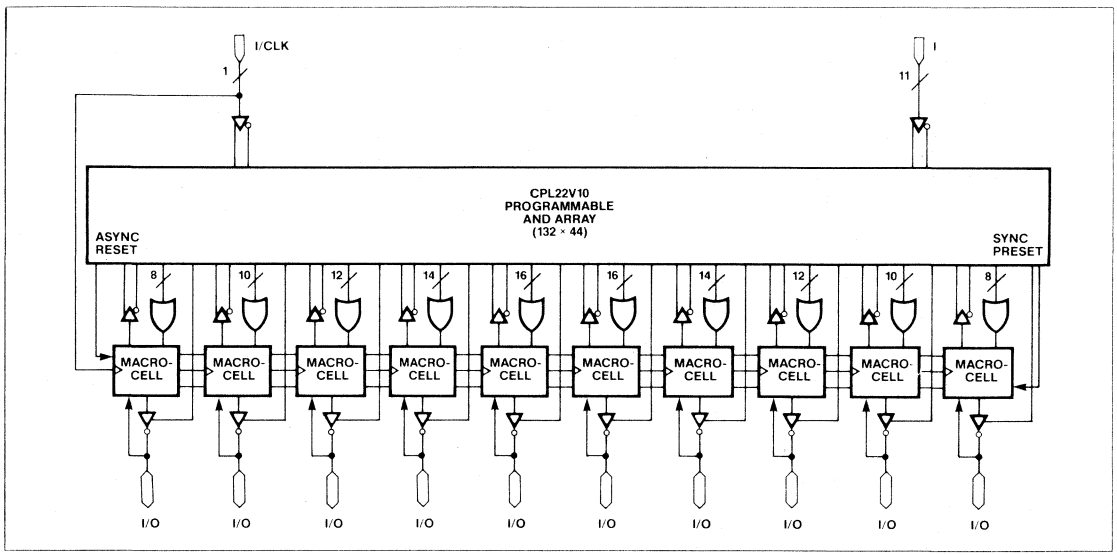


Dual In-Line Package



Plastic Leaded Chip Carrier

Figure 1. Block Diagram



The block diagram of the CPL22V10 device is shown in Figure 1. There are 12 dedicated inputs and 10 programmable macrocell outputs, which also serve as inputs. In addition, pin 1 acts either as a clock for each of the D-type registers or as another input. Each input and its complement is connected to a programmable AND array which contains a total of 120 product terms. Specifically, 8, 10, 12, 14, or 16 product terms drive each OR gate, which subsequently drives an output macrocell.

CONFIGURABLE OUTPUT MACROCELLS

One of the CPL22V10's unique features is its 10 user-configurable output macrocells. Each macrocell is programmed on an individual basis to provide one of four output configurations: combinatorial active low, combinatorial active high, registered active low, or registered active high as in Figure 2. Each output configuration is achieved by the programming of two additional bits (B0 and B1) as shown in Figure 3. Bit B1 controls whether the output will be registered or combinatorial, and bit B0 controls the output polarity, either active high or active low. These programmable functions are specified by the user in the design file specification during the design process.

When a registered output is chosen, the signal is shifted out on the positive clock transition to the I/O pin and also fed back into the array, providing current status information to the programmable array. This is important for state machine applications. When a combinatorial output is chosen or when the output is disabled and the signal is on the I/O pin, the signal is also fed back into the array. Note that the appropriate feedback path changes with the output mode.

PROGRAMMABLE OUTPUT ENABLE

Also associated with each of the 10 outputs in the CPL22V10 is an output enable (OE) product term, connected to the three-state output buffer. The OE product term can be implemented to represent any function of device inputs and output feedback combinations. As a result, each output can be selected as a bi-directional input/output or an output with feedback, when the buffer is enabled. Each output can be used as an input, when the buffer is disabled.

VARIABLE PRODUCT TERM DISTRIBUTION

The CPL22V10 not only provides an increased number of product terms on average, from eight in previous generation PLDs to the current 12 per output, but also provides variable product term distribution. The actual product term distribution varies from eight to sixteen, with one set of 8, 10, 12, 14, or 16 product terms available to each OR gate. This provides an advantage to the user who can now efficiently optimize his/her design to fit higher complexity functions or applications.

Figure 2. Configuration Options

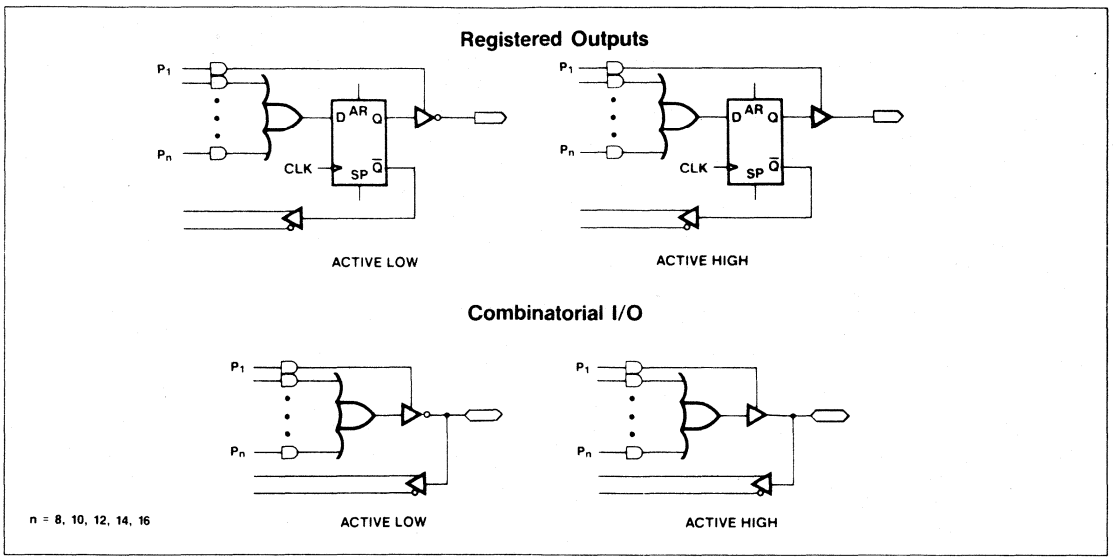
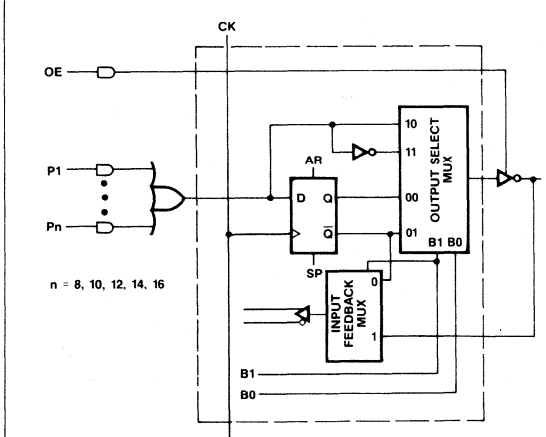


Figure 3. Output Macrocell with Configuration Bits



B_1	B_0	Output Macrocell Configuration
0	0	Registered/Active Low Output
0	1	Registered/Active High Output
1	0	Combinatorial/Active Low Output
1	1	Combinatorial/Active High Output

PROGRAMMABLE PRESET/RESET CONTROL

The final two product terms in the CPL22V10 device are used for RESET and PRESET control operations, and are shared among all ten output macrocell registers for easy system initialization. These product terms can be implemented to represent any product of device inputs and output feedbacks. When the Asynchronous Reset (AR) product term is asserted, the register of each macrocell will be forced low, independent of the clock signal. When the synchronous PRESET product term (SP) is asserted, the register of each macrocell will be forced high after the low-to-high clock transition. Depending on the output polarity chosen, the actual device outputs may be low or high.

POWER-UP RESET

During system power-up, each register in the CPL22V10 will be reset to a logic low, to ensure predictable system initialization. Actual output states, however, will be low or high, depending on the polarity chosen at each output. For reliable resets, the V_{CC} rise must be monotonic and the clock input must not change for 1μs.

SECURITY BIT

To prevent a proprietary CPL22V10 design from being copied without authorization, a security bit has been provided. The security bit is programmed via the designer's logic programmer. Once this is done, the read, verify, and preload operations are disabled, which completely secures the device. Also, since the CPL22V10 does not have visible fuses, enhanced security is offered over what is available on bipolar 22V10s.

TEST FEATURES

Register Preload

To ease functional testing, the CPL22V10 device is equipped with a register preload feature that allows an arbitrary state value to be loaded into any or all of its registers from the output pins. This makes it possible to check and verify any logical state transition, without having to run through an entire test vector sequence. Also, by using register preload, all possible states can be tested to guarantee proper in-system operation.

Test Array

Another feature of the CPL22V10 is the on-chip test array which increases device reliability by allowing each product term to be tested. The test array is programmed by Samsung to verify final functional and AC yields of the packaged device before shipping. When using the test array to test the device (even if the security bit has been programmed), only the input terms in the shaded portion of the functional block diagram are accessed. During normal operation, the test arrays are not accessed. As a result, the test array facilitates simple and shortened testing.

Input Term Testing

Finally, the CPL22V10 has additional product terms, one on output 14 and the other on output 23, which are controlled by the device's input terms. These product terms allow testing of all input structures and are programmed for functional and AC testing of the packaged device, before shipping. The additional product terms are not accessed as part of the normal operation. Having both input term testing and test arrays allows Samsung to provide a packaged device of the highest quality.

ERASURE (windowed-CERDIP only)

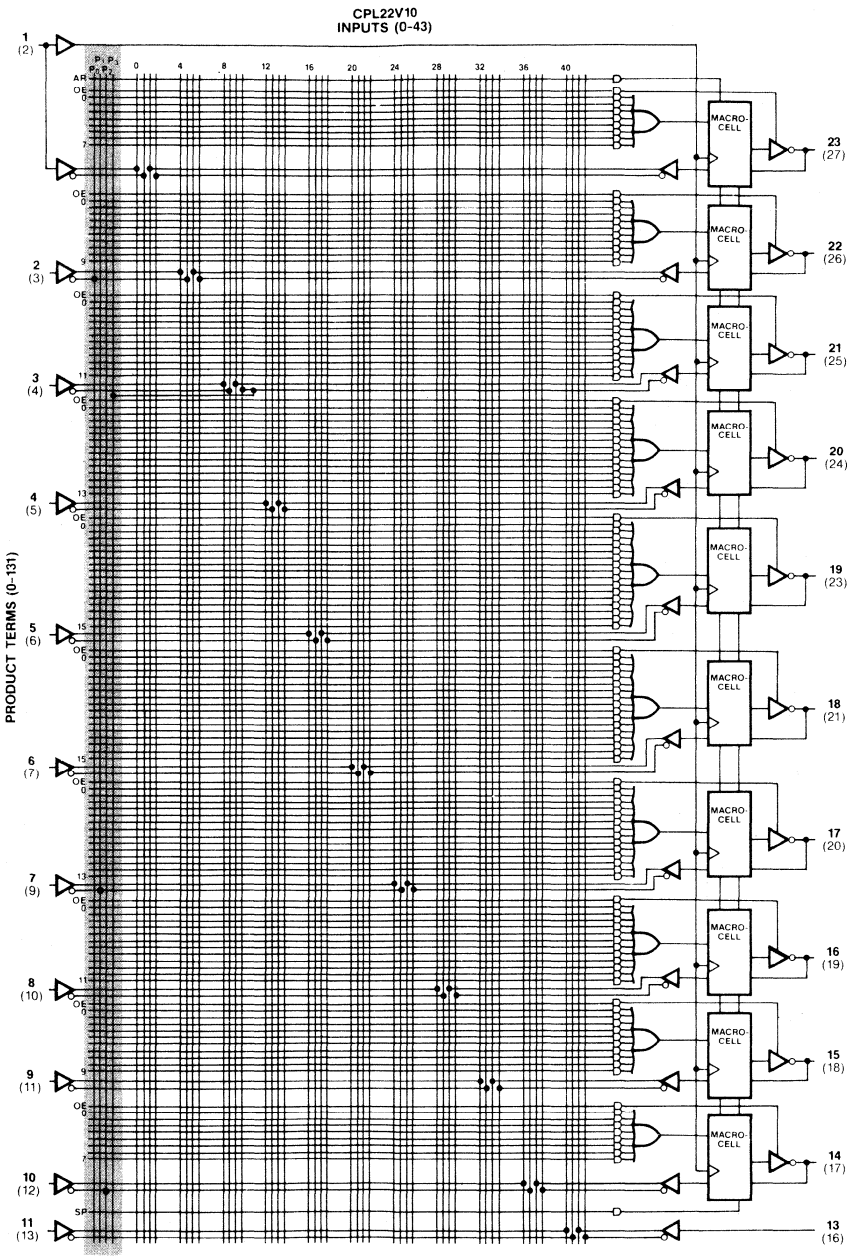
The CPL devices will erase by light at wavelengths of under 4000 Angstroms. The window must be covered by an opaque label to prevent erasure by exposure to sunlight or fluorescent lighting.

Recommended dose of ultraviolet light for erasure:

Wavelength of 2537 Angstroms
(minimum dose — 25Wsec/cm^2)

If an ultraviolet lamp with a 12mW/cm^2 power rating is used, 30 to 35 minutes of erasure time will suffice. The lamp must be closer than 1 inch from the window to guarantee optimal erasing conditions. Exposure to high intensity UV light for an extended period of time may cause permanent damage to the CPL devices. The maximum dosage recommended is 7250 Wsec/cm^2.

CPL22V10 FUNCTIONAL LOGIC DIAGRAM
DIP AND PLCC PINOUTS



3

CPL22V10 Absolute Maximum Ratings (Note 1)

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{CC}	-0.5 to +7.0	V
DC Input Voltage	V_{IN} ($\|I_{IN}\| \leq$ 20mA)	-3.0 to +7.0	V
Off-State DC Output Voltage	V_O	-0.5 to V_{CC} + 0.5	V
DC Programming Voltage	V_{PP}	14.0	V
Storage Temperature	T_{STG}	-65 to +150	°C
Power Dissipation per Package	P_D (Note 2)	500	mW

Note 1: Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only, and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

Note 2: Power dissipation temperature derating:
Plastic Package (N): -12mW/°C from 65°C to 85°C
Ceramic Package (J): -12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{CC}	4.5 to 5.5	V
DC Input and Output (Off-State) Voltages	V_{IN}, V_O (Note 3)	0 to V_{CC}	V
Operating Temperature Range, Commercial	T_A	0 to +70	°C

Note 3: Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND).

DC Electrical Characteristics (Over Recommended Operating Conditions)

Parameter	Symbol	Test Conditions			Min	Max	Unit
Low Level Input Voltage	V_{IL}	(Note 4)				0.8	V
High Level Input Voltage	V_{IH}	(Note 4)			2.0		V
Input Current	I_{IN}	$0 < V_{IN} < V_{CC}$			-10	10	μA
Low Level Output Voltage	V_{OL}	V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA			0.5	V
High Level Output Voltage	V_{OH}	V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	I_{OH} = -3.2mA		2.4		V
Off-State Output Leakage Current	I_{OZ}	V_{CC} = Max	$V_{SS} \leq V_O \leq V_{CC}$		-40	40	μA
Power Supply Current	I_{CC}	V_{IN} = GND, I_{OUT} = 0mA	V_{CC} = MAX	"L" STD		55 90	mA

Note 4: These are absolute values with respect to device ground. The applied voltage plus overshoots due to system and/or tester noise must not exceed these worst-case values.

Capacitance

Parameter	Description	Test Conditions	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1MHz		5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1MHz		8	

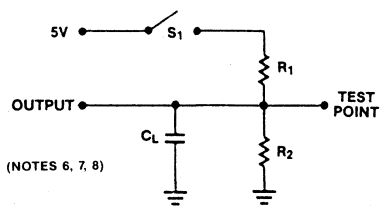
CPL22V10 AC Electrical Characteristics

Over Recommended Operating Conditions (Note 5)

Parameter	Symbol	-25		-35		Unit
		Min	Max	Min	Max	
Input or Feedback to Non-Registered Output	t_{PD} (Note 8)		25		35	ns
Clock to Registered Output or Feedback	t_{CO}		15		25	ns
Input to Output Enabled	t_{PZX}		25		35	ns
Input to Output Disabled	t_{PXZ}		25		35	ns
Setup Time from Input Feedback, or SP to Clock	t_{SU}	15		30		ns
Hold Time	t_H	0		0		ns
Clock Pulse Width (High or Low)	t_W	15		25		ns
Clock Period (t_{SU} + t_{CO})	t_P	30		55		ns
Maximum Frequency	f_{MAX}	33.3		18		MHz
Asynchronous Reset to Registered Output	t_{RO}		25		35	ns
Asynchronous Reset Pulse Width	t_{AW}	25		35		ns
Asynchronous Reset Recovery Time	t_{AR}	25		35		ns
Synchronous Preset Recovery Time	t_{SR}	25		35		ns

Note 5: Input rise and fall times (10% to 90% of V_{CC}): $t_r = t_f \leqq 6ns$

AC Test Circuit



Resistor Values (Ω)

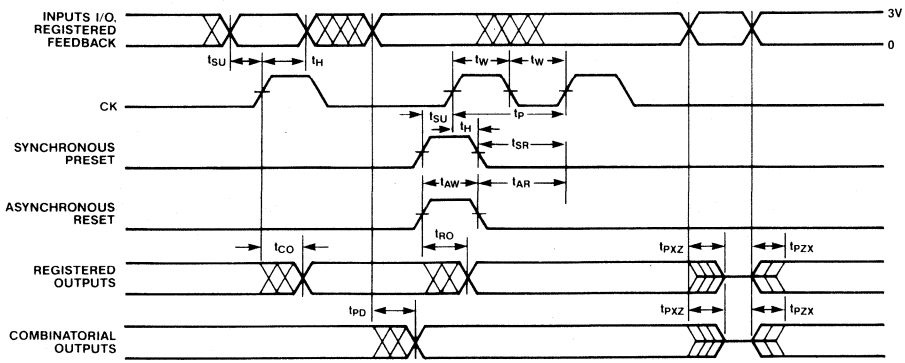
R1	R2
238	170

Note 6: C_L includes load and test jig capacitance.

Note 7: t_{PD} is tested with switch S_1 closed and C_L = 50pF.

Note 8: For 3-State outputs, output enable times are tested with C_L = 50pF to the 1.5V level; S_1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. Output disable times are tested with C_L = 5pF. HIGH to high impedance tests are made to an output voltage of V_{OH} - 0.5V with S_1 open; LOW to high impedance tests are made to the V_{OL} = 0.5V level with S_1 closed.

Switching Waveforms



Product Guide	*1*
Technical Overview/Quality and Reliability	*2*
Product Specifications	*3*
CPL Programming Electrical Specifications	*4*
CPL Starter Kit/CPL Programmer and Software Guide	*5*
Definition of Terms	*6*
Package Drawings	*7*
Sales Offices	*8*

Programming Samsung's CMOS PLDs

Samsung's CPL (CMOS programmable logic) devices use an EPROM programming technology which emphasizes complete testability (100% programming, functional, and AC) and high performance. Testability is inherent to the technology because it allows devices to be programmed and reprogrammed many times. High performance is achieved using a two-transistor EPROM cell which optimizes the speed of both read and write transistors. This results in CPL devices being as fast as many of their bipolar counterparts, and since they are fully tested prior to delivery to the customer, they provide higher programming yields.

Samsung's CPL devices are programmed using high voltage pulses, from 100 microseconds to 10 milliseconds in duration, which produce about 50 mA of programming current. At one time, eight to ten EPROM cells are programmed, depending on the device.

CPL EPROM cells are programmed by charging a floating gate with electrons and unprogrammed by irradiating the cells with ultraviolet (UV) light, making complete testing of all circuitry possible before shipping. (Bipolar parts, which use fuse cells, on the other hand, can be programmed only once, making 100% AC testing impossible.) By using special on-chip test arrays, additional functional and AC testing of CPL devices can also be performed without having to program the devices. Also, if the devices are contained in windowed packages, they may be programmed and erased, at the customer site a number of times, allowing the designer to test, develop, and fine-tune his/her logic without having to replace each programmed device.

CPL 20 Series (CPL16L8, CPL16R4, CPL16R6, CPL16R8)

The critical AC and DC parameters for programming the CPL 20 series devices are listed in Tables 1 and 2. The minimum and maximum parameter values are given for an ambient temperature of 25°C.

The pin configuration for programming the CPL 20 series parts is given in Figure 1. Notice that pin 1 is now called Vpp. It is raised to a programming voltage, Vpp, during programming (see Table 1). In this mode, pins 2 - 9 are used for addressing each location to be programmed and pins 12 - 19 are used for supplying data. Pin 11, the PGM/~OE pin, is the READ/WRITE pin in the programming mode. When it is raised to the programming voltage, Vpp, a write occurs and the data on the output pins is written into the addressed array locations. When it is switched to a logic LOW, a read occurs and the contents of the addressed locations can be checked or verified. When pin 11 is switched to a logic HIGH, the device is inhibited and the outputs go into a high impedance (Z) state.

The CPL devices are programmed one byte at a time for a total of 256 (32 input terms, 8 wide) bytes of memory. This memory can be addressed once the array is programmed. The addresses are selected via pins 2 - 9 (A0 - A7). Pins 2 - 4 select one of eight product terms (or outputs) as shown in Table 3, whereas pins 5 - 9 select one of 32 input terms according to Table 4. The test input terms can be selected, as in Table 5, by raising pin 7 to Vpp and entering the test programming mode of operation. Here, the duplicated memory cells of the test array are addressed at the same locations as the 0, 1, 2, and 3 product terms. (The test arrays, having 32 bytes of memory, are provided for the purpose of post-assembly testing and are disconnected in normal operation.)

Parameter	Description	Min.	Max.	Units
V_{PP}	Programming Voltage	13.0	14.0	V
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IH}	Input High Voltage	3.0		V
V_{IL}	Input Low Voltage		0.4	V
V_{OH} (1)	Output High Voltage	2.4		V
V_{OL} (1)	Output Low Voltage		0.4	V
I_{PP}	Supply Current		50	mA

(1) During verify operation

Table 1. DC Programming Parameters (at 25°C)

Parameter	Description	Min.	Max.	Units
t_{PP} (2)	Programming Pulse Width	100	10,000	µS
$t_{AS,OS}$	Setup Time	1.0		µS
$t_{AH,DH}$	Hold Time	1.0		µS
t_r, t_f (2)	V_{PP} Rise and Fall Time	1.0		µS
t_{VD}	Delay to Verify	1.0		µS
t_{VP}	Verify Pulse Width	2.0		µS
t_{DV}	Verify to Data Valid	20.0		µS
t_{DZ}	Verify to High Z		1.0	µS

(2) Measured at 10% and 90% votage levels

Table 2. AC Programming Parameter (at 25°C)

Selecting the address pins 2 - 9, whether in the normal or test modes, leaves one byte of cells available for programming. The data to be programmed is sent via data inputs D0 - D7 to every 8th product term (in groups of 8: 0, 8, 16, 24, 32, 40, 48, and 56). Note that there is a one-to-one correlation between each data input and its respective product term. For example, a "1" on data input D0 programs product term 0, a "1" on data input D1 programs product term 8, etc. After each byte of cells is programmed, the product term decoder (pins 2 - 4) is incremented by one, until all 64 product terms are addressed. As a result, each of the input terms is addressed eight times. After verification, the input term decoder (pins 5 - 9) is incremented by one and the sequence repeated 32 times.

In the unprogrammed state, each input is connected to each product term. When a logic level HIGH on a data line is presented during programming, the memory cell is disconnected from the selected input term and product term (like a blown fuse using bipolar technology). During the verify operation, which can be used to check if the part is blank or is correctly programmed, an unprogrammed cell causes a logic level HIGH to appear on the output, and a programmed cell causes a logic level LOW to appear on the output. A summary of the programming operating modes with appropriate pin assignments for Samsung's CPL 20 series devices is shown in Table 6. The corresponding programming waveforms for the standard array and for the test array are shown in Figures 2 and 3. The waveforms for securing the logic of the CPL20X parts is illustrated in Figure 4, whereas the waveforms for verifying that the parts are secured (unable to read back programmed information) are shown in Figure 5. Note that the security bit is programmed using a single 10 ms pulse (pin 11).

Finally, the actual sequence that is used to program the standard and test memory cells is described in the form of a flowchart in Figure 6.

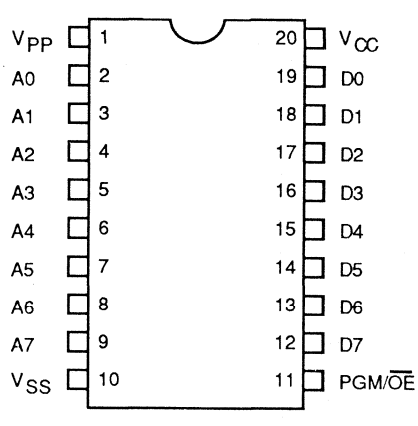


Figure 1. CPL20 Programming Pin Configuration

Product Term Line Number								Pin Number		
								2	3	4
0	8	16	24	32	40	48	56	L	L	L
1	9	17	25	33	41	49	57	H	L	L
2	10	18	26	34	42	50	58	L	H	L
3	11	19	27	35	43	51	59	H	H	L
4	12	20	28	36	44	52	60	L	L	H
5	13	21	29	37	45	53	61	H	L	H
6	14	22	30	38	46	54	62	L	H	H
7	15	23	31	39	47	55	63	H	H	H
D0	D1	D2	D3	D4	D5	D6	D7			
Data Inputs, Pins 12 through 19										

L = V_{IL} or 0.4V Max.
H= V_{IH} or 3.0V Min.

Table 3. Product Term Address Decodes for CPL20 Family

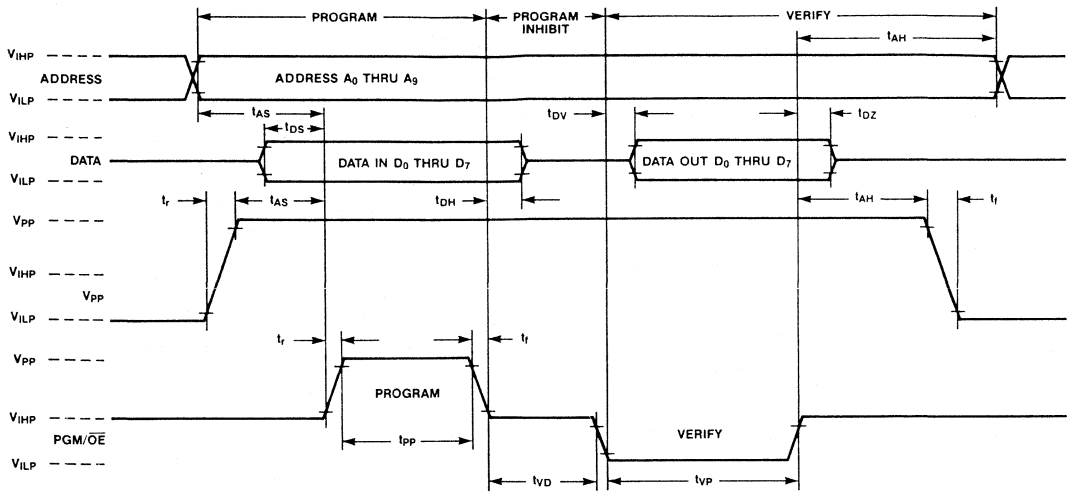


Figure 2. Programming Waveforms Normal Array

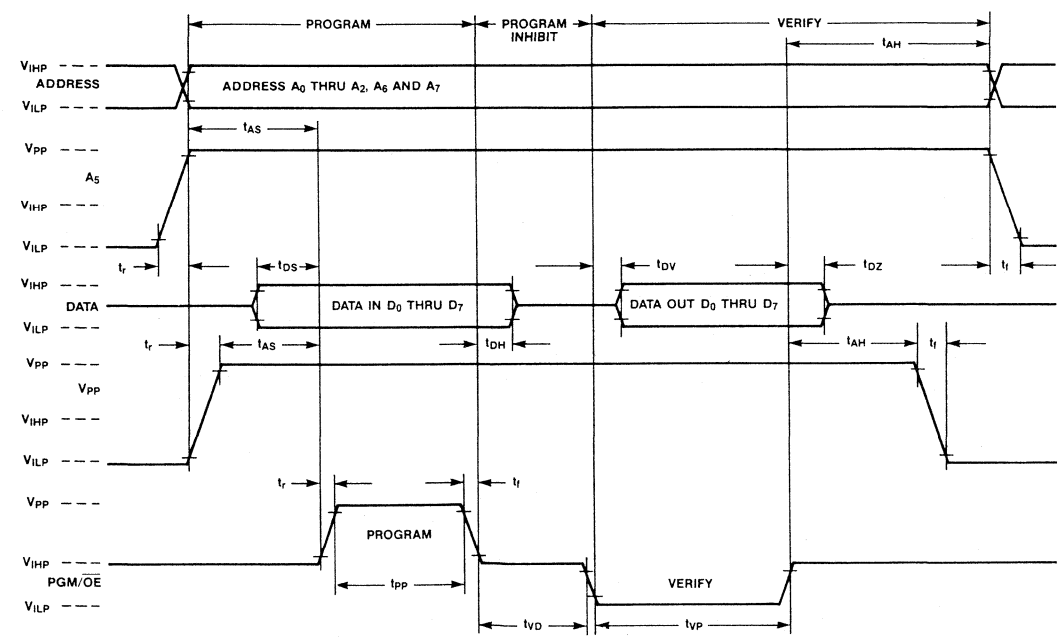


Figure 3. Program Waveforms Test Array

Input Term Line Number	Pin Number				
	5	6	7	8	9
0	L	L	L	L	L
1	H	L	L	L	L
2	L	H	L	L	L
3	H	H	L	L	L
4	L	L	H	L	L
5	H	L	H	L	L
6	L	H	H	L	L
7	H	H	H	L	L
8	L	L	L	H	L
9	H	L	L	H	L
10	L	H	L	H	L
11	H	H	L	H	L
12	L	L	H	H	L
13	H	L	H	H	L
14	L	H	H	H	L
15	H	H	H	H	L

Input Term Line Number	Pin Number				
	5	6	7	8	9
16	L	L	L	L	H
17	H	L	L	L	H
18	L	H	L	L	H
19	H	H	L	L	H
20	L	L	H	L	H
21	H	L	H	L	H
22	L	H	H	L	H
23	H	H	H	L	H
24	L	L	L	H	H
25	H	L	L	H	H
26	L	H	L	H	H
27	H	H	L	H	H
28	L	L	H	H	H
29	H	L	H	H	H
30	L	H	H	H	H
31	H	H	H	H	H

$L = V_{IL}$ or 0.4V Max.
$H = V_{IH}$ or 3.0V Min.

Table 4. Input Term Address Decodes for CPL20 Family

Test Term Line Number	Pin Number		
	7	8	9
P0	V_{PP}	L	L
P1	V_{PP}	H	L
P2	V_{PP}	L	H
P3	V_{PP}	H	H

$L = V_{IL}$ or 0.4V Max.
$H = V_{IH}$ or 3.0V Min.

Table 5. Test Term Address Decodes for CPL20 Family

Operating Mode \ Pin Name / Pin Number	V_{PP} 1	PGM/ $\overline{OE}$ 11	A0 2	A1 3	A2 4	A3 5	A4 6	A5 7	A6 8	A7 9	D9 - D0 12 - 19
Regular PAL Logic (1)	CK/HL	HL	HL	HL	HL	HL	HL	HL	HL	HL	Logic Function Out
Program PAL	V_{PP}	V_{PP}	A	A	A	A	A	A	A	A	Program Data In
Program Inhibit	V_{PP}	V_{IH}	X	X	X	X	X	X	X	X	High Z
Program Verify	V_{PP}	V_{IL}	A	A	A	A	A	A	A	A	Programmed Data Out
Test PAL Logic (1)	CK/X	X	HL	HL	HL	X	V_{PP}	X	X	X	Logic Function Out
Program Test PAL (3)	V_{PP}	V_{PP}	A	A	A	X	X	V_{PP}	A	A	Program Data In
Program Test Inhibit (3)	V_{PP}	V_{IH}	A	A	A	X	X	V_{PP}	A	A	High Z
Program Test Verify (3)	V_{PP}	V_{IL}	A	A	A	X	X	V_{PP}	A	A	Programmed Data Out
Program Security Bit	V_{PP}	V_{PP}	X	V_{PP}	X	X	X	X	X	X	High Z
Verify Security Bit	X	X	X	(2)	V_{PP}	X	X	X	X	X	High Z
Register Preload	X	X	X	X	X	V_{PP}	X	X	X	X	Data Input to Register

(1) See data sheet for actual I /O configuration
(2) Pin 3 = V_{OL} ; Data security is in effect
Pin 3 = V_{OH} ; Data is unsecured and may be accessed
(3) Pin 7 selects the test mode of operation and must be taken to V_{PP} before selecting test program operation with pin 1 taken to V_{PP}

HL = TTL logic Input level
A = Address input level
X = Don't care ; GND < X < V_{CC}
V_{IL} = 0.4V (Max.)
V_{IH} = 3.0 V (Min.)
V_{PP} = 13.5V (13.0 v - 14.0 V)

Table 6. CPL20 Programming Operating Modes

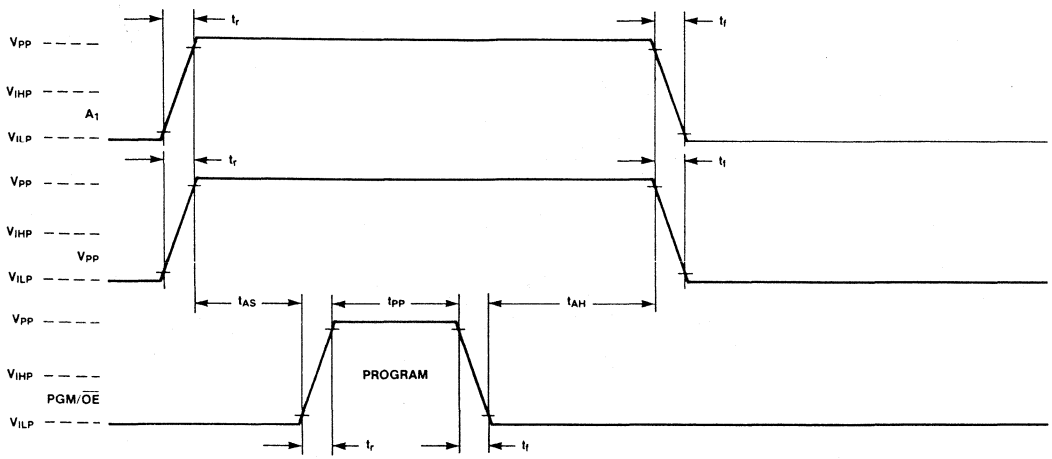


Figure 4. Activating Program Security

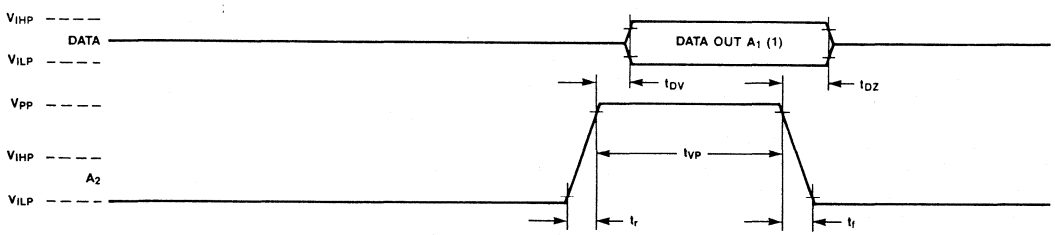


Figure 5. Verify Program Security

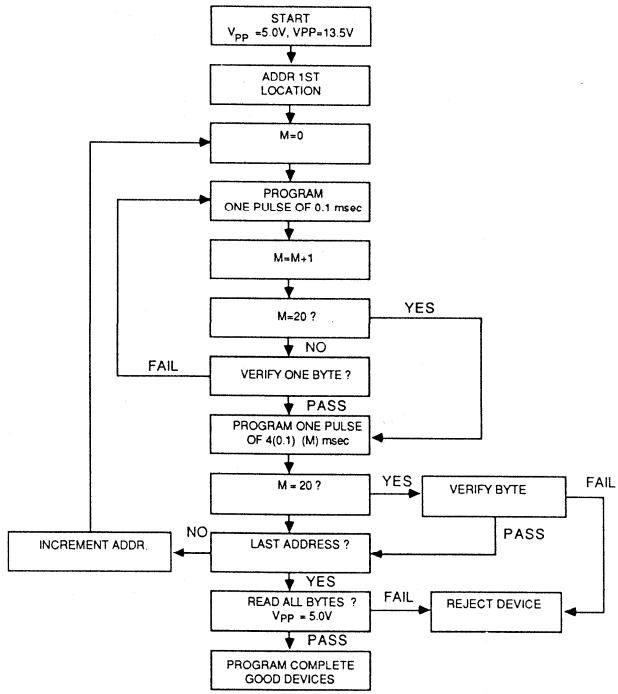


Figure 6. CPL20 Programming Flow Chart

CPL 24 Series

(CPL20L10, CPL20L8, CPL20R4, CPL20R6, CPL20R8)

The critical AC and DC parameters for programming the CPL 24 series devices are listed in Tables 7 and 8. The minimum and maximum parameter values are given for an ambient temperature of 25°C.

The pin configuration for programming the CPL 24 series parts is given in Figure 7. Notice that pin 1 is now called Vpp. It is raised to a programming voltage, Vpp, during programming (see Table 7). In this mode, pins 2 - 11 are used for addressing each location to be programmed and pins 14 - 23 are used for supplying data. Pin 13, the PGM/ ~OE pin, is the READ/WRITE pin in the programming mode. When it is raised to the programming voltage, Vpp, a write occurs and the data on the output pins is written into the addressed array locations. When it is switched to a logic LOW, a read occurs and the contents of the addressed locations can be checked or verified. When pin 13 is switched to a logic HIGH, the device is inhibited and the outputs go into a high impedance (Z) state.

Parameter	Description	Min.	Max.	Units
V_{PP}	Programming Voltage	13.0	14.0	V
V_{CC}	Supply Voltage During Programming	4.75	5.25	V
V_{IH}	Programming Input High Voltage	3.0		V
V_{IL}	Programming Input Low Voltage		0.4	V
V_{OH}(1)	Output High Voltage	2.4		V
V_{OL} (1)	Output Low Voltage		0.4	V
I_{PP}	Programming Supply Voltage		50	mA

(1) During verify operation

Table 7. DC Programming Parameters (at 25°C)

Parameter	Description	Min.	Max.	Units
t_{PP} (2)	Programming Pulse Width	100	10,000	µS
t_{AS}, t_{DS}	Setup Time	1.0		µS
t_{AH}, t_{DH}	Hold Time	1.0		µS
t_r t_f (2)	V_{PP}Rise and Fall Time	1.0		µS
t_{VD}	Delay to Verify	1.0		µS
t_{VP}	Verify Pulse Width	2.0		µS
t_{DV}	Verify to Data Valid	20.0		µS
t_{DZ}	Verify to High Z		1.0	µS

(2) Measured at 10% and 90% votage levels

Table 8. AC Programming Parameter (at 25°C)

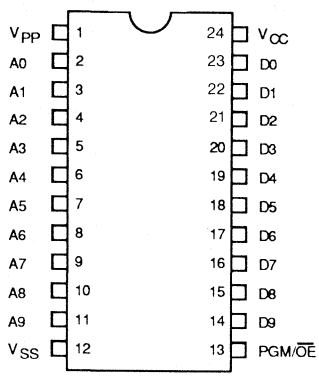


Figure 7. CPL24 Programming Pin Configuration

All of the CPL 24 pin devices, except the CPL20L10, are programmed one byte at a time for a total of 256 bytes of memory. The CPL20L10 is programmed 10 bits at a time for a total of 128 x 10 bits of memory. The memory can be addressed once the array is programmed. The addresses are selected via pins 2 - 11 (A0 - A9). Specifically, pins 2-4 select one of eight product terms (or pins 8 and 9 select one of four product terms for the CPL20L10) for each output as shown in Tables 9A and 9B, whereas pins 5-10 (or pins 2-7 for the CPL20L10) select one of 32 input terms as shown in Table 10. The test input terms can be selected, as in Table 11, by raising pin 7 to Vpp and entering the test programming mode of operation. Here, the duplicated memory cells of the test array are addressed at the same locations as the 0, 1, 2, and 3 product terms. (The test arrays are provided for the purpose of post- assembly testing and are disconnected in normal operation.)

Product Term Line Number								Pin Number		
								2	3	4
8	16	24	32	40	48	56	64	L	L	L
9	17	25	33	41	49	57	65	H	L	L
10	18	26	34	42	50	58	66	L	H	L
11	19	27	35	43	51	59	67	H	H	L
12	20	28	36	44	52	60	68	L	L	H
13	21	29	37	45	53	61	69	H	L	H
14	22	30	38	46	54	62	70	L	H	H
15	23	31	39	47	55	63	71	H	H	H

L = V_{IL} or 0.4V Max.
H= V_{IH} or 3.0V Min.

Table 9A. Product Term Address Decodes for CPL24 Family, except CPL20L10

Product Term Line Number										Pin Number	
										8	9
0	8	16	24	32	40	48	56	64	72	L	L
1	9	17	25	33	41	49	57	65	73	H	L
2	10	18	26	34	42	50	58	66	74	L	H
3	11	19	27	35	43	51	59	67	75	H	H

L = V_{IL} or 0.4V Max.
H= V_{IH} or 3.0V Min.

Table 9B. Product Term Address Decodes for CPL20L10

Input Term Line Number	Pin Number					
	5/2*	6/3*	7/4*	8/5*	9/6*	10/7*
0	L	L	L	L	L	L
1	H	L	L	L	L	L
2	L	H	L	L	L	L
3	H	H	L	L	L	L
4	L	L	H	L	L	L
5	H	L	H	L	L	L
6	L	H	H	L	L	L
7	H	H	H	L	L	L
8	L	L	L	H	L	L
9	H	L	L	H	L	L
10	L	H	L	H	L	L
11	H	H	L	H	L	L
12	L	L	H	H	L	L
13	H	L	H	H	L	L
14	L	H	H	H	L	L
15	H	H	H	H	L	L
16	L	L	L	L	H	L
17	H	L	L	L	H	L
18	L	H	L	L	H	L
19	H	H	L	L	H	L
20	L	L	H	L	H	L
21	H	L	H	L	H	L
22	L	H	H	L	H	L
23	H	H	H	L	H	L
24	L	L	L	H	H	L
25	H	L	L	H	H	L
26	L	H	L	H	H	L
27	H	H	L	H	H	L
28	L	L	H	H	H	L
29	H	L	H	H	H	L
30	L	H	H	H	H	L
31	H	H	H	H	H	L
32	L	L	L	L	L	H
33	H	L	L	L	L	H
34	L	H	L	L	L	H
35	H	H	L	L	L	H
36	L	L	H	L	L	H
37	H	L	H	L	L	H
38	L	H	H	L	L	H
39	H	H	H	L	L	H

*CPL20L10 only

L = V_{IL} or 0.4V Max.
H= V_{IH} or 3.0V Min.

Table 10. Input Term Address Decodes for CPL24 Family

Selecting the address pins 2 - 11, whether in the normal or test modes, leaves one byte of cells (or 10 bits for the CPL20L10) available for programming. The data to be programmed is sent via data inputs D1 - D8 to every 8th product term (in groups of 8: 8, 16, 24, 32, 40, 48, 56, and 64 or 0, 8, 16, 24, 32, 40, 48, 56, 64, and 72 for the CPL20L10). Note that there is a one-to-one correlation between each data input and its respective product term. For a CPL20L8, for example, a "1" on data input D1 programs product term 8, a "1" on data input D2 programs product term 16, etc. After each byte of cells is programmed, the product term decoder (pins 8 - 10) is incremented by one until all 64 (40) product terms are addressed. As a result, each of the product terms is addressed eight (four) times. After verification, the input decoder (pins 2 - 7) is incremented by one and the sequence repeated 32 times.

In the unprogrammed state, each input is connected to each product term. When a logic level HIGH on a data line is presented during programming, the memory cell is disconnected from the selected input term and product term (like a blown fuse using bipolar technology). During the verify operation, which can be used to check if the part is blank or correctly programmed, an unprogrammed cell causes a logic level HIGH to appear on the output, and a programmed cell causes a logic level LOW to appear on the output.

A summary of the programming operating modes with appropriate pin assignments for Samsung's CPL24 series devices is shown in Table 12. The corresponding programming waveforms for the standard array and for the test array are shown in Figures 8 and 9. The waveforms for securing the logic of the CPL24 parts are illustrated in Figure 10, whereas the waveforms for verifying that the parts are secured (unable to read back programmed information) are shown in Figure 11. Note that the security bit is programmed using a single 10 milliseconds pulse (pin 13).

Finally, the actual sequence that is used to program the standard and test memory cells is described in the form of a flowchart in Figure 12.

Test Term Line Number	Pin Number		
	8/4*	9/5*	7
P0	L	L	V_{PP}
P1	H	L	V_{PP}
P2	L	H	V_{PP}
P3	H	H	V_{PP}

* CPL20L10 only

L = V_{IL} or 0.4V Max.
H= V_{IH} or 3.0V Min.

Table 11. Test Term Address Decodes for CPL24 Family

Operting Mode \ Pin Name / Pin Number	V_{PP} 1	PGM/~OE 13	A0 2	A1 3	A2 4	A3 5	A4 6	A5 7	A6 8	A7 9	A8 10	A9 11	D9 - D0 14-23
Regular PAL Logic (1)	CK/HL	HL	HL	HL	HL	HL	HL	HL	HL	HL	HL	HL	Logic Function Out
Program PAL	V_{PP}	V_{PP}	A	A	A	A	A	A	A	A	A/X(5)	X	Program Data In
Program Inhibit	V_{PP}	V_{IH}	X	X	X	X	X	X	X	X	X	X	High Z
Program Verify	V_{PP}	V_{IL}	A	A	A	A	A	A	A	A	A/X(5)	X	Programmed Data Out
Test PAL Logic (1)	CK/X	X	HL	HL/X(5)	HL/X(5)	X	V_{PP}	X/HL(5)	X	X	X/HL(5)	X	Logic Function Out
Program Test PAL (3)	V_{PP}	V_{PP}	A/X(5)	A/X(5)	A	X/A(5)	X	V_{PP}	A	A	X/A(5)	X	Program Data In
Program Test Inhibit (3)	V_{PP}	V_{IH}	A/X(5)	A/X(5)	A	X/A(5)	X	V_{PP}	A	A	X/A(5)	X	High Z
Program Test Verify (3)	V_{PP}	V_{IL}	A/X(5)	A/X(5)	A	X/A(5)	X	V_{PP}	A	A	X/A(5)	X	Programmed Data Out
Program Security Bit	V_{PP}	V_{PP}	X	V_{PP}	X	X	X	X	X	X	X	X	High Z
Verify Security Bit	X	X	X	(2)	V_{PP}	X	X	X	X	X	X	X	High Z
Program output polarity	V_{PP}	V_{PP}	X	X	X	X	X	X	X	V_{PP}	X	X	High Z
Verify output polarity	X	X	X	X	X	X	X	X	X	(4)	V_{PP}	X	High Z
Register Preload (6)	X	X	X	X	X	V_{PP}	X	X	X	X	X	X	Data Input to Register

(1) See data sheet for actual I /O configuration
(2) Pin 3 = V_{OL} ; Data security is in effect
Pin 3 = V_{OH} ; Data is unsecured and may be accessed
(3) Pin 7 selects the test mode of operation and must be taken to V_{PP} before selecting test program operation with pin 1 taken to V_{PP}
(4) Pin 9 = V_{OL} ; Erased bit asserted low at output
(5) For CPL20L10 only
(6) For registered parts only.

HL = TTLlogic Input level
A = Address input level
X = Don't care ; GND < X < VCC
V_{IL} = 0.4V (Max.)
V_{IH} = 3.0 V (Min.)
V_{PP} = 13.5V (13.0 v - 14.0 V)

4

Table 12. CPL24 Programming Operating Modes

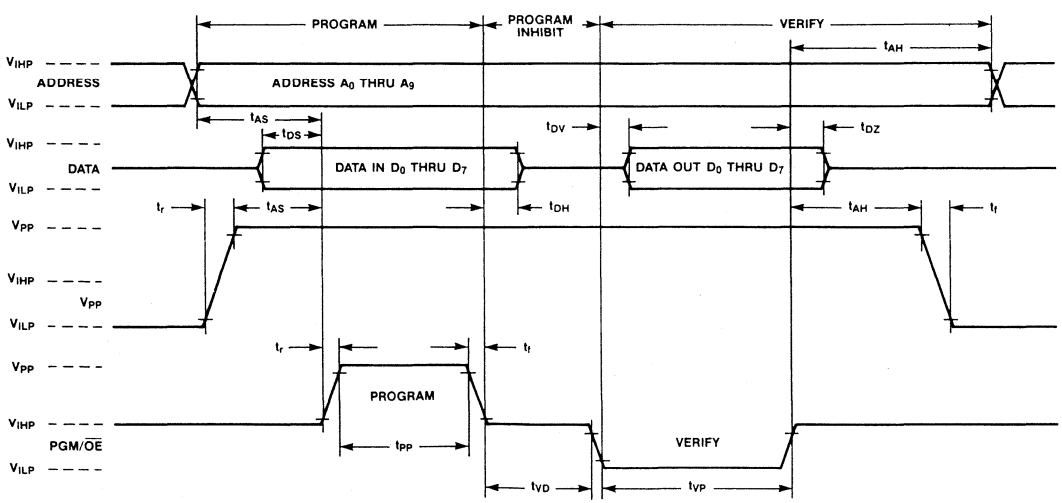


Figure 8. Programming Waveforms Normal Array

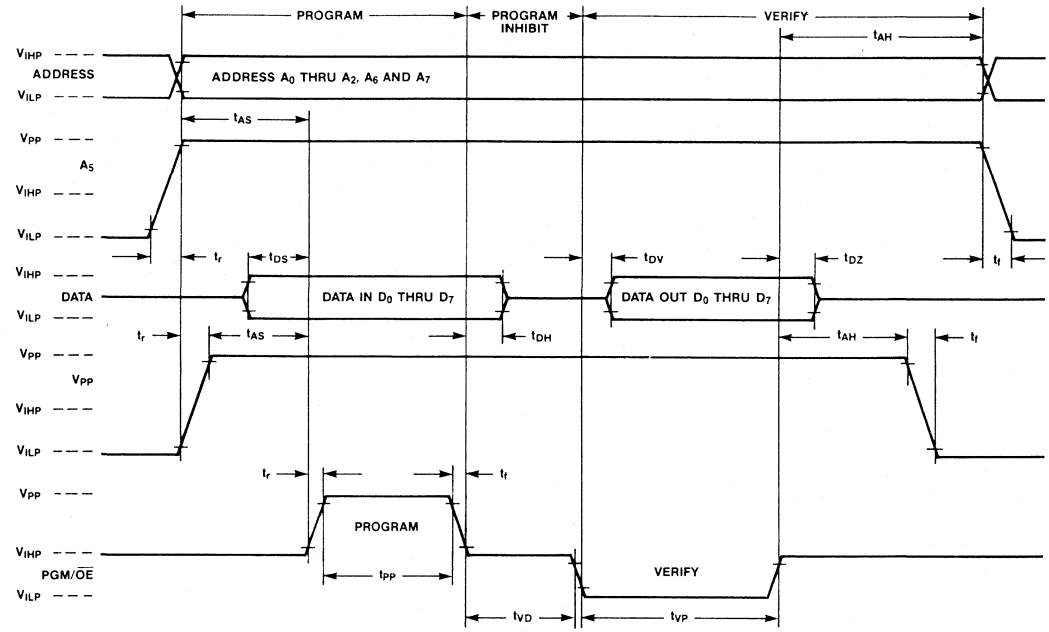


Figure 9. Program Waveforms Test Array

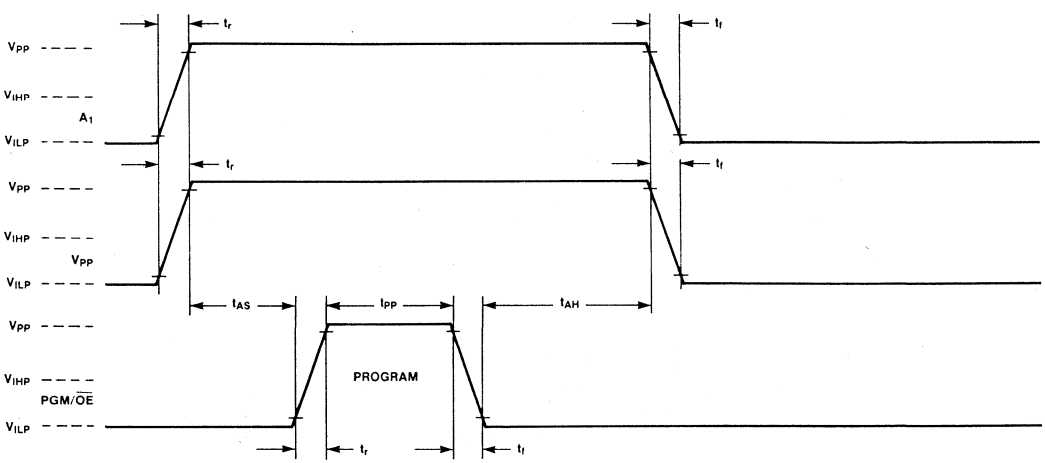


Figure 10. Activating Program Security

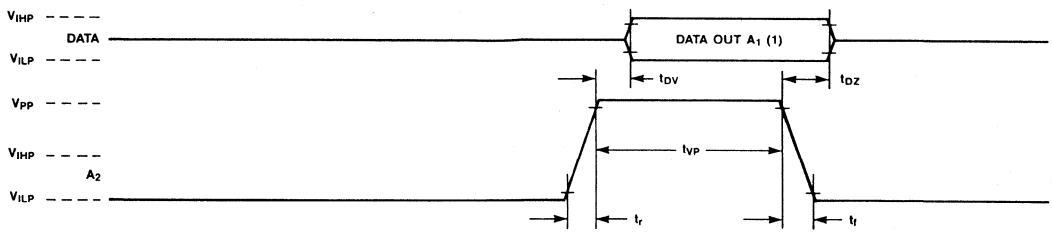


Figure 11. Verify Program Security

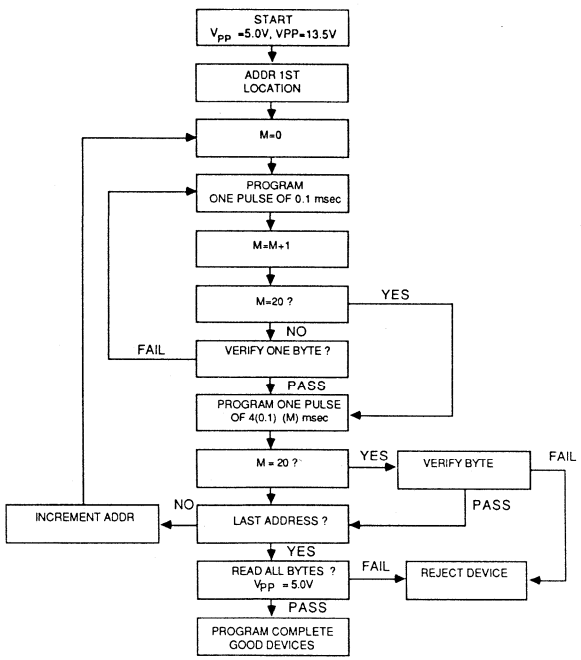


Figure 12. CPL24 Programming Flowchart

CPL22V10, CPL16V8 and CPL20V8 programming electrical specifications are also available. For more information, please contact the factory at (800) 669--5400.

Product Guide 1

Technical Overview/Quality and Reliability 2

Product Specifications 3

CPL Programming Electrical Specifications 4

CPL Starter Kit/CPL Programmer and Software Guide 5

Definition of Terms 6

Package Drawings 7

Sales Offices 8

CPL STARTER KIT

The new and convenient CPL Starter Kit, jointly developed with Personal CAD Systems, includes a newly updated software package developed by Logical Devices, Inc. and is based on CUPL™, the most powerful high-level language for designing programmalbe logic. It also includes samples of Samsung CPL devices, the CPL data book and tutorial material.

The starter kit contains everything needed to develop complete prototypes. Unlike bipoar PAL devices, CPL devices are reprogrammable and this simplifies prototype development.

CPL devices are programmed with standard PLD programmers. The design cycle (shown in the flowchart below) is short, because design, programming and test can all be done at the designer's desk. Modifications are implemented in minutes, and hardware wiring changes can be reduced to a minimum.

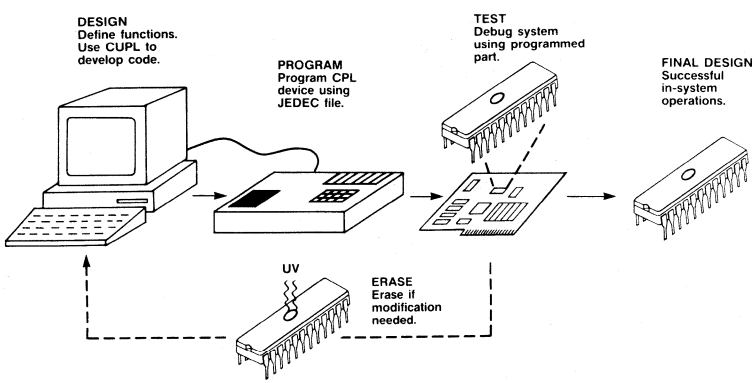
A variety of options are available for entering designs including truth tables (for designing decoders); state diagrams and ASM flowcharts (for describing sequential designs); and high-level equations (which support string substitution and are used to describe any design).

CUPL™ power tools provide logic minimization, available in three algorithms for improved optimization. DeMorganization (helpful when negating complex expressions) and simulation are also provided to help verify logic designs.

Design documentation is comprehensive. CUPL offers a logic "template" file for design ease; a fuse map and expanded product-term information; a chip diagram illustrating pin assignments; and a symbol table of all variables. An excellent software manual is provided, and Personal CAD Systems offers customer support.

The CPL Starter Kit contains:

- CPL20, CPL24, CPL16V8, CPL20V8 and CPL22V10 samples
- A CPL Data Book
- A CUPL™ Software Manual
- A Programmable Logic User's Guide (PLUG) diskette, which lets the user browse interactively through the workings of programmable logic.
- "My First PAL Design", a booklet that leads the user step-by-step through programmable logic design



CPL DESIGN CYCLE

PROGRAMMER INFORMATION

The following programmer vendors supply hardware and related software that support Samsung's CPL (CMOS Programmable Logic) devices. The hardware and software revisions listed for each vendor are the earliest revisions which incorporate the CPL product family.

Later software and hardware revisions can also be assumed to support the CPL family. For the latest system/software revisions, please contact the vendor directly. Please note that some vendors also require adapters and modules to be installed before programming the devices.

VENDOR	FAMILY	PART #	DEVICE CODE	SYSTEM/REV	MODULE	ADAPTER
ADAMS MCDONALD ENT. PROMAC Division 800 Airport Road Monterey, CA 93940 Tel: (408)373-3651	CPL20	CPL16L8 CPL16R4 CPL16R6 CPL16R8		Sprint Plus/ Rev V3.2G		
				PROMAC P11/ Rev 2.01		
	CPL24	CPL20L8 CPL20R4 CPL20R6 CPL20R8 CPL20L10		Sprint Plus/ Rev V3.2G		
				PROMAC P11/ Rev 2.01		
ADVANCED PROGRAMMING SYSTEMS 35623 Chaplin Drive Fremont, CA 94536 Tel: (415)796-0682	CPL20	CPL16L8 CPL16R4 CPL16R6 CPL16R8		University Programmer	PLD1 Module	
	CPL24	CPL20L8 CPL20R4 CPL20R6 CPL20R8 CPL20L10		University Programmer	PLD1 Module	
ADVIN SYSTEMS 1050-L East Duane Sunnyvale, CA 94086 Tel: (408)984-8600	CPL20	CPL16L8 CPL16R4 CPL16R6 CPL16R8		Sailor PAL/ Rev 8.7		
	CPL24	CPL20L8 CPL20R4 CPL20R6 CPL20R8 CPL20L10		Sailor PAL/ Rev 8.7		
BP MICROSYSTEMS 1061 Haddington #190 Houston, Texas 77043 Tel: (713)461-9430 (800) 225-2102	CPL20	CPL16L8 CPL16R4 CPL16R6 CPL16R8		PLD 1100/ Version 1.10		
	CPL24	CPL20L8 CPL20R4 CPL20R6 CPL20R8		PLD1100/ Version 1.16		
		CPL20L10		PLD 1100/ Version 1.10		

CPL PROGRAMMER INFORMATION (Continued)

VENDOR	FAMILY	PART #	DEVICE CODE	SYSTEM/REV	MODULE	ADAPTER
DATA I/O CORPORATION 10525 Willow Road N.E. P.O. Box 97064 Redmond, WA 98073-9764 Tel: (800)247-5700 Tel: (206)881-6444	CPL20	CPL16L8 CPL16R4 CPL16R6 CPL16R8	9D17 9D24 9D24 9D24	Unisite 40/ Rev 1.7		
				Model 60A/H Rev 12		360A-001
				Models 19, 29A, 29B	Logic Pak/ Version 4	303A-011A/ Version 4
	CPL24	CPL20L8 CPL20R4 CPL20R6 CPL20R8 CPL20L10	9D26 9D27 9D27 9D27 9D06	Unisite 40/ Rev 2.2		
				Model 60A/H Rev 13 (4)		360A-001
				Models 19, 29A, 29B	Logic Pak/ Version 4	303A-011A/ Version 7
	2nd Gen CPL	CPL22V10	9D28	Unisite 40/ Rev 2.5		
				Model 60A/H Rev 14		360A-001
				Models 19, 29A, 29B	LogicPak/ Version 4	360A-011A Version 9
DIGELEC, INC. 22736 Vanowen St. Canoga Park, CA 91307 Tel: (818)887-3755 Tel: (800) 367-8750	CPL20	CPL16L8 CPL16R4 CPL16R6 CPL16R8		Model 860/ Rev 1.2		
	CPL24	CPL20L8 CPL20R4 CPL20R6 CPL20R8 CPL20L10		Model 860/ Rev. 1.4		
INLAB 2150-1 W 6th Avenue Broomfield, CO 80020 Tel: (303) 460-0103	CPL20	CPL16L8 CPL16R4 CPL16R6 CPL16R8		Model 28A/U Rev 9.0 Model 28A/L Rev 9.0		
	CPL24	CPL20L8 CPL20R4 CPL20R6 CPL20R8		Model 28A/U Rev 9.07 Model 28A/L Rev 9.07		
		CPL20L10		Model 28A/U Rev 9.0 Model 28A/L Rev 9.0		
KONTRON CORPORATION 630 Clyde Avenue Mountain View, CA 94039 Tel: (415)965-7020 Tel: (800)227-8834 KONTRON MESSTECHNIK GMBH Oskar-von-Miller Str.1.1 9057 ECHING/W. Germany Tel: (08165) 77-0	CPL20	CPL16L8 CPL16R4 CPL16R6 CPL16R8	9D17 9D24 9D24 9D24	MPP-80 or EPP-80	UPM-B/C Rev. 2.2	
	CPL24	CPL20L8 CPL20R4 CPL20R6 CPL20R8 CPL20L10	9D26 9D27 9D27 9D27 9D06	MPP-80 or EPP-80	UPM-B/C Rev 2.3	

5

CPL PROGRAMMER INFORMATION (Continued)

VENDOR	FAMILY	PART #	DEVICE CODE	SYSTEM/REV	MODULE	ADAPTER
LOGICAL DEVICES 1201 N.W. 65th Place Ft. Lauderdale, FL 33309 Tel: (305)974-0967	CPL20	CPL16L8 CPL16R4 CPL16R6 CPL16R8		Husky/Rev 2.0 AllPro/Rev 1.47C PALPro 2X/8X- Rev 4.2 Gang Pro		
	CPL24	CPL20L8 CPL20R8 CPL20R6 CPL20R8 CPL20L10		AllPro/Rev 1.47C PALPro 2X/8X- Rev 4.3 Gang Pro		
OLIVER ADVANCED ENGINEERING 320 West Arden St. Glendale, CA 91203 Tel: (818)240-0080	CPL20	CPL16L8 CPL16R4 CPL16R6 CPL16R8		Omni 28/ Omni 40/ Omni 60/ Rev 1.0		
	CPL24	CPL20L8 CPL20R4 CPL20R6 CPL20R8 CPL20L10		Omni 28/ Omni 40/ Omni 60/ Rev 2.0		
RED SQUARE (DIGITAL MEDIA) 11770 Warner Avenue Suite 225 Fountain Valley, CA 92708 Tel: (714) 751-1373	CPL20	CPL16L8 CPL16R4 CPL16R6 CPL16R8		Uniwriter (IQ180)/Rev 3.2 Uniwriter (1Q280)/Rev 3.3		
	CPL24	CPL20L8 CPL20R4 CPL20R6 CPL20R8 CPL20L10		Uniwriter (IQ180)/Rev 3.3 Uniwriter (IQ280)/Rev 3.3		
RETNEL SYSTEMS P.O. Box 1348 Lawrence, MA 01842 Tel: (508) 683-4659	CPL20	CPL16L8 CPL16R4 CPL16R6 CPL16R8		ZAP-A-PAL Rev 2.8		
	CPL24	CPL20L8 CPL20R4 CPL20R6 CPL20R8 CPL20L10		ZAP-A-PAL Rev 2.8		
STAG MICROSYSTEMS 1600 Wyatt Drive, Ste 3 Santa Clara, CA Tel: (408)988-1118	CPL20	CPL16L8 CPL16R4 CPL16R6 CPL16R8	65029 65032 65031 65030	ZL30/Rev 26 ZL30A/Rev 26 PPZ/Rev 30	ZM2200	
STAG ELECTRONIC DESIGNS, LTD. Nortons Building Bridge Road East Welwyn Garden City Herts, England Tel: (0707) 325136	CPL24	CPL20L8 CPL20R4 CPL20R6 CPL20R8 CPL20L10	65056 65059 65058 65057 65060	ZL30/Rev 31 (10) ZL30A/Rev 31 PPZ/Rev 37 (10)	 ZM2200	
	2nd Gen CPL	CPL22V10	65061	ZL30/Rev 33 ZL30A/Rev 33 PPZ/Rev 39		

CPL PROGRAMMER INFORMATION (Continued)

VENDOR	FAMILY	PART #	DEVICE CODE	SYSTEM/REV	MODULE	ADAPTER
SUNRISE ELECTRONICS 524 S. Vermont Avenue Glendora, CA 91740 Tel: (818) 914-1926	CPL20	CPL16L8 CPL16R4 CPL16R6 CPL16R8		Z1000B Universal Programmer Rev 4.0		
	CPL24	CPL20L8 CPL20R4 CPL20R6 CPL20R8 CPL20L10		Z1000B Universal Programmer Rev 4.0		
VARIX 1210 E. Campbell Road Richardson, TX 75081 Tel: (214) 437-0777	CPL20	CPL16L8 CPL16R4 CPL16R6 CPL16R8		SP0300 (Omni Programmer)/ Rev 5.1		
	CPL24	CPL20L8 CPL20R4 CPL20R6 CPL20R8 CPL20L10		TBD		
WITTS ASSOCIATES 42 Matuk Drive Hyde Park, NY 12538 Tel: (914) 229-5189	CPL20	CPL16L8 CPL16R4 CPL16R6 CPL16R8		PAL-PLUS Rev 1.01		
	CPL24	CPL20L8 CPL20R4 CPL20R6 CPL20R8 CPL20L10				

5

DEVELOPMENT SYSTEM SUPPORT FOR CPL20 FAMILY

The development software used for generating a logic file (JEDEC file) for programming CPL devices is listed below. These software programs also provide logic simulation.

ABEL™

DATA I/O CORPORATION
10525 Willows Road, N.E.
P.O. Box 97046
Redmond, WA 98073-9746

Tel: (206) 881-6444

CUPL™

PERSONAL CAD SYSTEMS, INC.
1290 Parkmoor Avenue
San Jose, CA 95126

Tel: (800) 523-5207
(800) 628-8748 (in California)

PLDesigner™

MINC, INC.
1575 York Road
Colorado Springs, CO 80918

Tel: (303) 590-1155

HP PLD Design System

HEWLETT-PACKARD CORPORATION
3000 Hanover
Palo Alto, CA 94304

Tel: (800) 752-0900

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CUPL™ is a trademark of Personal CAD Systems, Inc.

Product Guide 1

Technical Overview/Quality and Reliability 2

Product Specifications 3

CPL Programming Electrical Specifications 4

CPL Starter Kit/CPL Programmer and Software Guide 5

Definition of Terms 6

Package Drawings 7

Sales Offices 8

DEFINITION OF TERMS

CLOCK FREQUENCY TERMS	
f_{MAX} =	*Maximum clock frequency* The highest clock input rate of a bistable circuit that can maintain stable logic level transitions at the output and produce correct output logic levels per the specification.
CURRENT TERMS	
I_{CC} =	*Supply current* The current which occurs at the V_{CC} supply terminal when the circuit is in operation.
I_{IN} =	*Input current* The current which occurs when voltage is applied to that input.
I_{OS} =	*Short-circuit output current* The current which occurs when the output is short- circuited to ground or other specified potential with input conditions applied which establish the output logic level farthest from ground or other specified potential.
I_{OZH} =	*High-level off-state output leakage current* The current which occurs on an output having three-state capability with high-level input voltage conditions applied to establish a high-impedance state at the output.
I_{OZL} =	*Low-level off-state output leakage current* The current which occurs on an output having three-state capability with low-level input voltage conditions applied to establish a high-impedance state at the output.
I_{PP} =	*Programming supply current* The current that is supplied when programming the device.
POWER TERMS	
P_D =	*Power dissipation per package* The amount of power consumed when the device is in operation.
TEMPERATURE TERMS	
T_{STG} =	*Storage temperature* Temperature at which devices can be stored without damage.
T_A =	*Operating (Ambient) Temperature* Temperature at which devices can be operated without damage.

DEFINITION OF TERMS (Continued)

TIME TERMS	
t_{CLK}=	*Clock to registered output or feedback* The length of time that elapses between when the clock switches and when the data on the registered output or feedback becomes valid.
t_{DV} =	*Verify to data valid* The length of time it takes for the data to become valid once the PGM/~OE pin goes to a low state during verify programming normal/test mode or address 2 goes to V_{PP} during verify program security mode.
t_{DZ} =	*Verify to high Z* The length of time it takes for the data to go into a high-impedance state once the PGM/~OE pin goes to a high state during verify programming normal/test mode or address 2 goes low during verify program security mode.
t_f =	*V_{PP} fall time* The length of time it takes for a signal to change from a high to low voltage state as measured between the leading and trailing edge of the pulse waveform.
t_H =	*Hold time* The length of time a signal must be retained at one input terminal after an active clock transition occurs at another input terminal.
t_P =	*Clock period* The length of time it takes for the clock to complete one high and low cycle.
t_{PP} =	*Programming pulse width* The length of time a signal stays at the programming voltage as measured between the leading and trailing edges of a pulse waveform.
t_{PD} =	*Propagation delay time* The time interval during which the non-registered output changes from one defined level (high or low) to the other defined level specified on the input and output voltage waveforms.
$t_{PXZ11,13}$ =	*Pin 11,13 to output disable* The propagation delay time between when pin 11,13 switches from a high to low state and when the three-state output changes from either a high or low state to a high- impedance (off) state.

DEFINITION OF TERMS (Continued)

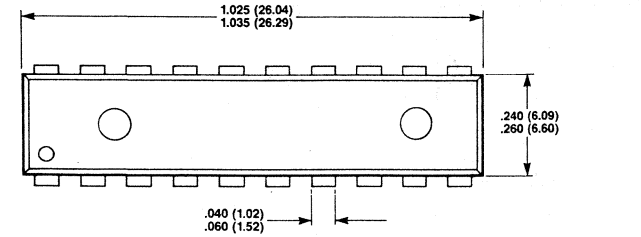
TIME TERMS (Continued)	
$t_{PZX11,13}$ =	*Pin 11,13 to output enable* The propagation delay time between when pin 11,13 switches from a low to high state and when the three-state output changes from a high-impedance (off) state to either a high or low state.
t_{PXZ} =	*Input to output disable* The propagation delay time between when a specified input switches and when the three-state output changes from a high or low state to a high-impedance (off) state.
t_{PXZ} =	*Input to output enable* The propagation delay time between when a specified input switches and when the three-state output changes from a high-impedance (off) state to a high or low state.
t_r =	*V_{PP} rise time* The length of time it takes for a signal to change from a low to high voltage state as measured between the leading and trailing edge of the pulse waveform.
t_{SU} =	*Set-up time from input or feedback to clock* The length of time a data signal must be maintained at one input terminal before a consecutive active clock transition at another input terminal can occur. (For R4, R6, and R8 parts only.)
t_{VD} =	*Delay to verify* The length of time the PGM/~OE pin stays high during program inhibit mode as measured between the leading and trailing edges of a pulse waveform.
t_{VP} =	*Verify pulse width* The length of time the PGM/~OE pin stays low during verify programming normal/test mode or stays at V_{PP} during verify program security mode as measured between the leading and trailing edges of a pulse wave form.
t_W =	*Clock or pulse width (high or low)* The length of time the signal stays high or low as measured between the leading and trailing edges of a pulse waveform.

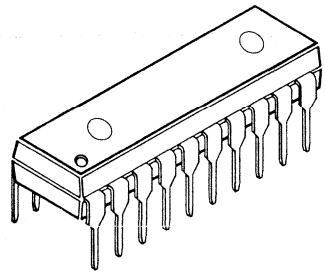
DEFINITION OF TERMS (Continued)

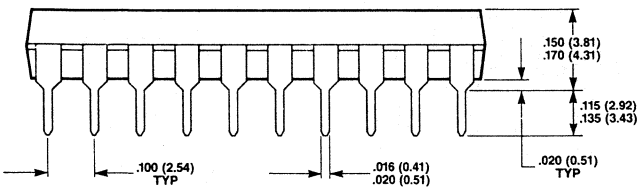
VOLTAGE TERMS	
V_{CC} =	*Supply voltage* The voltage needed to operate the circuit with respect to ground.
V_{IH} =	*High-level input voltage* An input voltage that is the lowest voltage still able to "turn-on" or enable logic.
V_{IL} =	*Low-level input voltage* An input voltage that is the lowest voltage still able to "turn-off" or disable logic.
V_{IN} =	*DC input voltage* The applied voltage range allowed on inputs.
V_{OH} =	*High-level output voltage* The output voltage produced when input conditions are applied which establish a high output level.
V_{OL} =	*Low-level output voltage* The output voltage produced when input conditions are applied which establish a low output level.
V_O =	*Off-State DC output voltage* The applied voltage range allowed on outputs in off-state mode.
V_{PP} =	*DC programming voltage* Voltage that must be applied to circuit in order to program it.

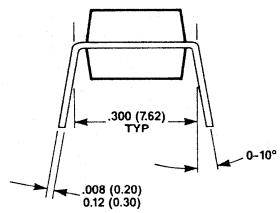
Product Guide	*1*
Technical Overview/Quality and Reliability	*2*
Product Specifications	*3*
CPL Programming Electrical Specifications	*4*
CPL Starter Kit/CPL Programmer and Software Guide	*5*
Definition of Terms	*6*
Package Drawings	*7*
Sales Offices	*8*

20 PIN PLASTIC DIP



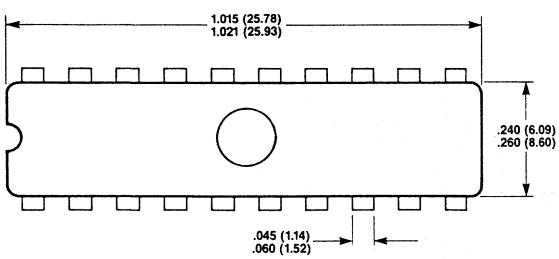


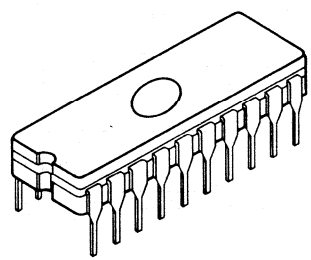


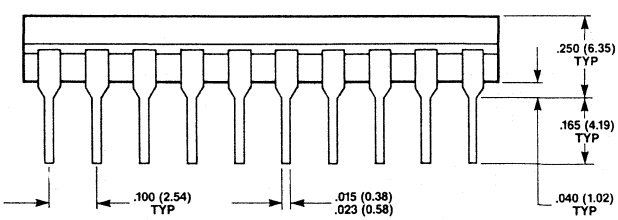


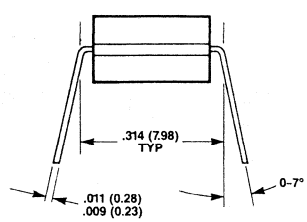
DIMENSIONS IN INCHES
AND (MILLIMETERS)
MIN.
MAX.

20 PIN WINDOWED CERDIP





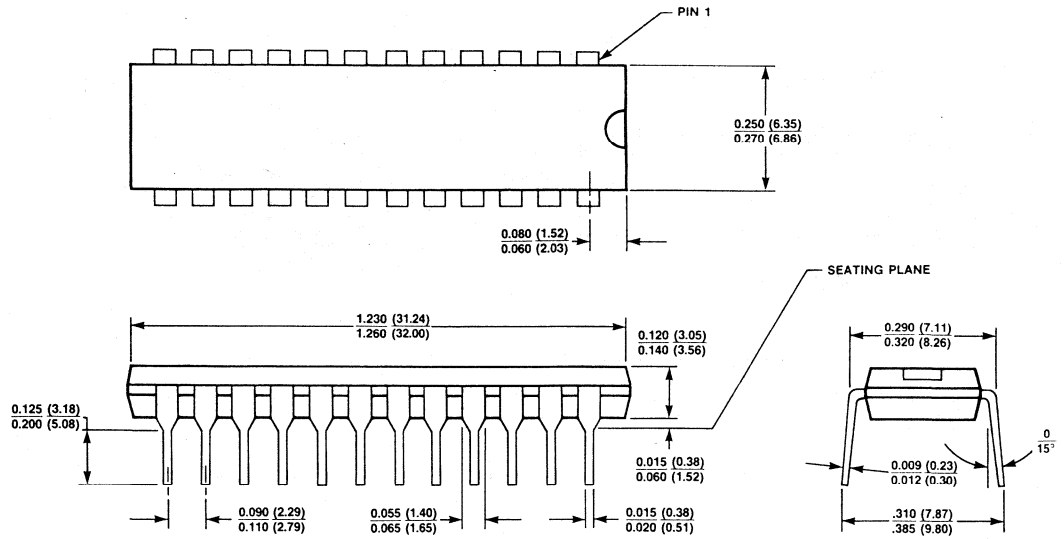




DIMENSIONS IN INCHES
AND (MILLIMETERS)
MIN.
MAX.

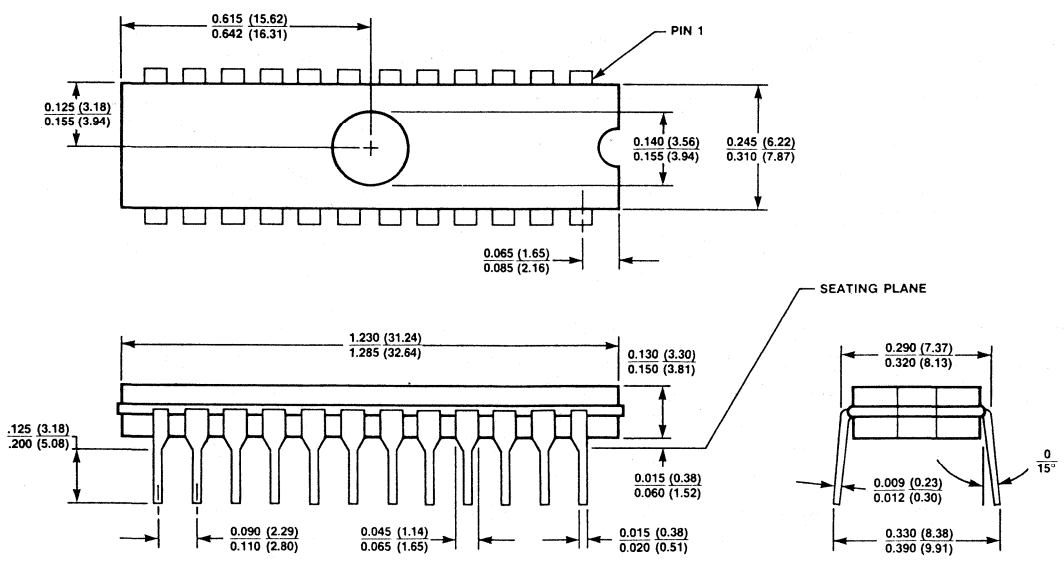
7

24 PIN PLASTIC DIP



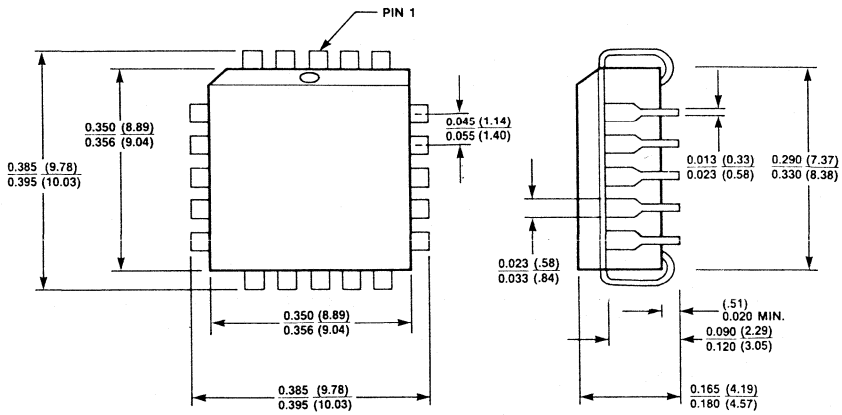
DIMENSIONS IN INCHES AND (MILLIMETERS)
MIN.
MAX.

24 PIN WINDOWED CERDIP



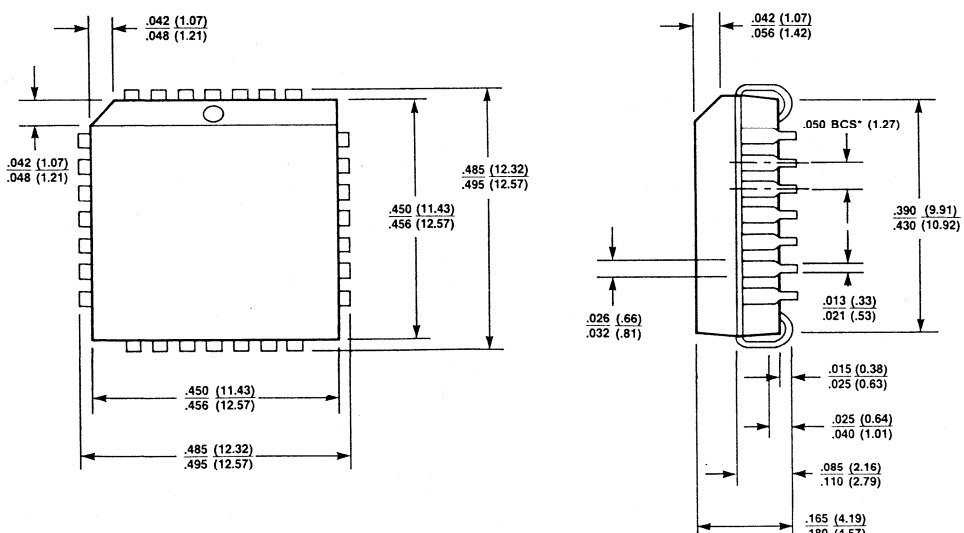
DIMENSIONS IN INCHES AND (MILLIMETERS)
MIN.
MAX.

20 PIN PLCC



DIMENSIONS IN INCHES AND (MILLIMETERS)
MIN.
MAX.

28 PIN PLCC



*BSC = BASIC SPACING BETWEEN CENTERLINES

DIMENSIONS IN INCHES AND (MILLIMETERS)
MIN.
MAX.

7

Product Guide 1

Technical Overview/Quality and Reliability 2

Product Specifications 3

CPL Programming Electrical Specifications 4

CPL Starter Kit/CPL Programmer and Software Guide 5

Definition of Terms 6

Package Drawings 7

Sales Offices 8

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U.S.A. and CANADA

ARIZONA

HAAS & ASSOC. INC. TEL: (602) 998-7195
77441 East Butherus Drive FAX: (602) 998-7869
Suite 300
Scottsdale,AZ 85260

CALIFORNIA

QUEST REP INC. TEL: (619) 565-8797
9444 Farnham St. FAX: (619) 565-8990
Suite 107
San Diego,CA 92123

SYNPAC TEL: (408) 988-6988
3945 Freedom Circle FAX: (408) 988-5041
Suite 650
Santa Clara,CA 95054

WESTAR REP COMPANY TEL:(714) 832-3325
2472 Chambers Road FAX: (714) 832-7894
Suite 100
Tustin, CA 92680

WESTAR REP COMPANY TEL: (213) 539-2156
25202 Crenshaw Blvd. FAX: (213) 539-2564
Suite 217
Torrance, CA 90505

CANADA

TERRIER ELEC. TEL: (416) 622-7558
145 The West Mall FAX: (416) 626-1035
Etobicoke, Ontario, Canada
M9C 1C2

TERRIER ELEC. TEL: (604) 433-0159
3700 Gilmore Way, 106A FAX: (604) 430-0144
Burnaby, B.C., Canada
V5G 4M1

TERRIER ELEC.
6600 Transcanadienne TEL: (514) 695-4421
Suite 750-17 FAX: (514) 695-3295
Pointe Claire, Quebec, Canada
H9R 452

COLORADO

CANDAL INC. TEL: (303) 935-7128
7500 West Mississippi Ave. FAX: (303) 935-7310
Suite A-2
Lakewood, CO 80226

CONNECTICUT

PHOENIX SALES TEL: (203) 496-7709
257 Main Street FAX: (203) 496-0912
Torrington,CT 06790

FLORIDA

MEC TEL: (305) 426-8944
700 W. Hillsboro Blvd. FAX: (305) 426-8799
Bldg. 4, Suite 204
Deerfield Beach, FL 33441

MEC TEL: (407) 332-7158
511 Carriage Road (407) 773-1100
Indian Harbour Beach, FL 32937 FAX: (407) 830-5436

MEC TEL: (407) 799-0820
830 North Atlantic Blvd. FAX: (407) 799-0923
Suite B401
Cocoa Beach, FL 32931

MEC TEL: (813) 522-3433
1001 45th, N.E. FAX: (813) 522-3993
St. Petersburg, FL 33703

ILLINOIS

IRI TEL: (312) 967-8430
8430 Gross Point Road FAX: (312) 967-5903
Skokie,IL 60076

INDIANA

STB & ASSOC. INC. TEL: (317) 844-9227
3003 E. 96th St. FAX: (317) 844-1904
Suite102
Indianapolis,IN 46240

MARYLAND

ADVANCED TECH SALES TEL: (301) 789-9360
809 Hammonds Ferry Rd. FAX: (301) 789-9364
Suite D
Linthicum,MD 21090

8

MASSACHUSETTS

NEW TECH SOLUTIONS, INC. TEL: (617) 229-8888
111 South Bedford Street FAX: (617) 229-1614
Suite 102
Burlington, MA 01803

MICHIGAN

JENSEN C.B. TEL: (313) 643-0506
2145 Crooks Rd. FAX: (313) 643-4735
Troy,MI 48084

MINNESOTA

IRI
1120 East 80th Street TEL: (612) 854-1120
Bloomington, MN 55420 FAX: (612) 854-8312

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NECCO TEL: (201) 461-2789
2460 Lemoine Avenue FAX: (201) 461-3857
Ft. Lee,NJ 07024

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S.W. SALES, INC. TEL: (505) 899-9005
7137 Settlement Way, N.W.
Albuquerque, NM 87120

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T-SQUARE TEL: (315) 463-8592
6443 Ridings Road FAX: (315) 463-0355
Syracuse, NY 13206

T-SQUARE TEL: (716) 924-9101
7353 Victor-Pittsford Road FAX: (716) 924-4946
Victor, NY 14564

NORTH CAROLINA

GODWIN & ASSOC. TEL: (919) 878-8000
1100 Logger Ct. FAX: (919) 878-3923
Suite B 102
Raleigh, NC 27609

GODWIN & ASSOCIATES TEL: (704)549-8500
2812 Oak Leigh Drive FAX: (704) 549-9792
Charlotte, NC 28213

OHIO

BAILEY, J.N. & ASSOC. TEL: (513) 687-1325
129 W. Main Street FAX: (513) 687-2930
New Lebanon,OH 45345

BAILEY, J.N. & ASSOC. TEL: (614) 262-7274
2679 Indianola Avenue FAX: (614) 262-0384
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